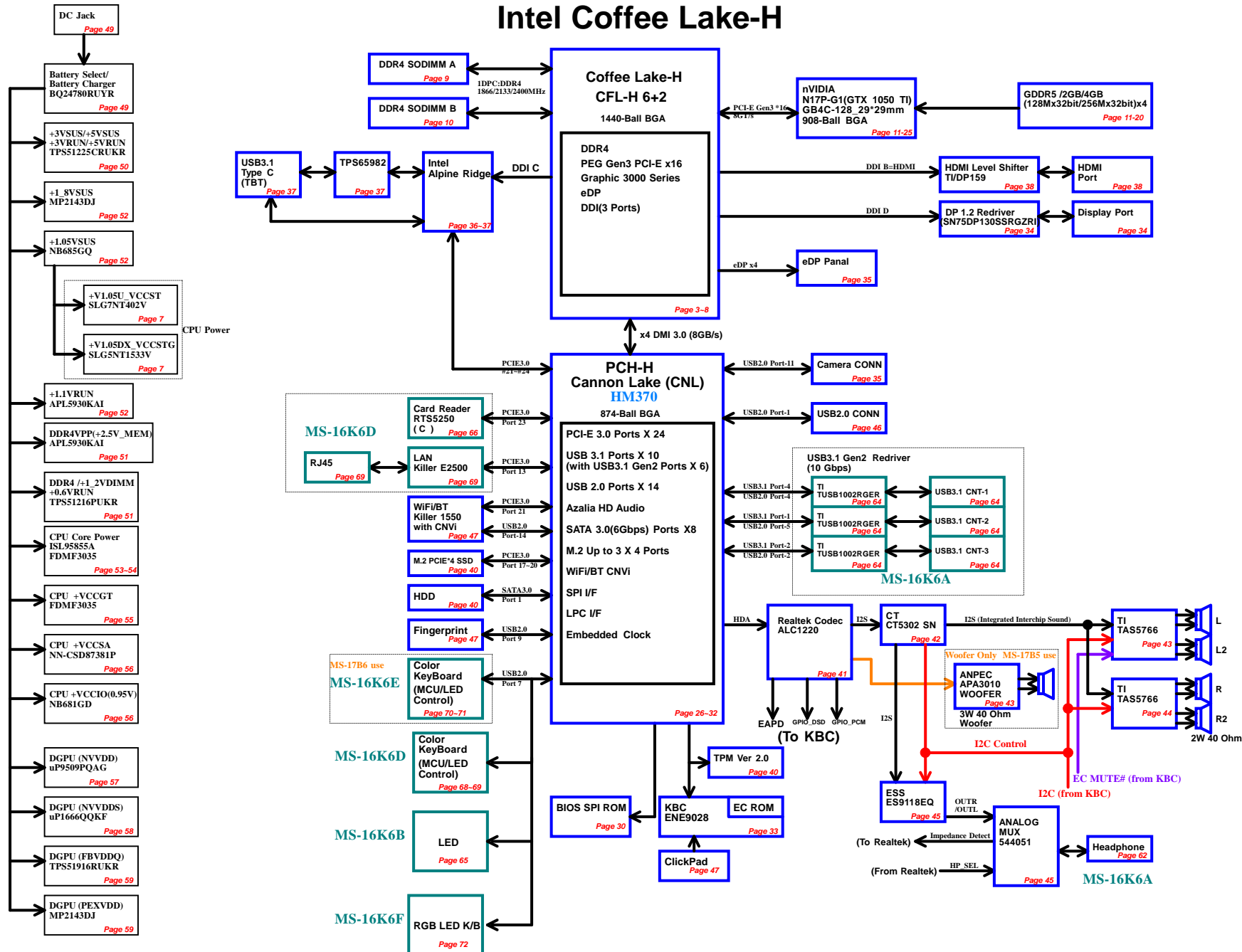
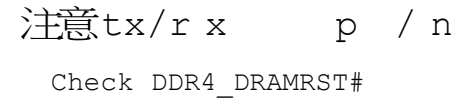


MS-16K6/17B6 Ver : 0A

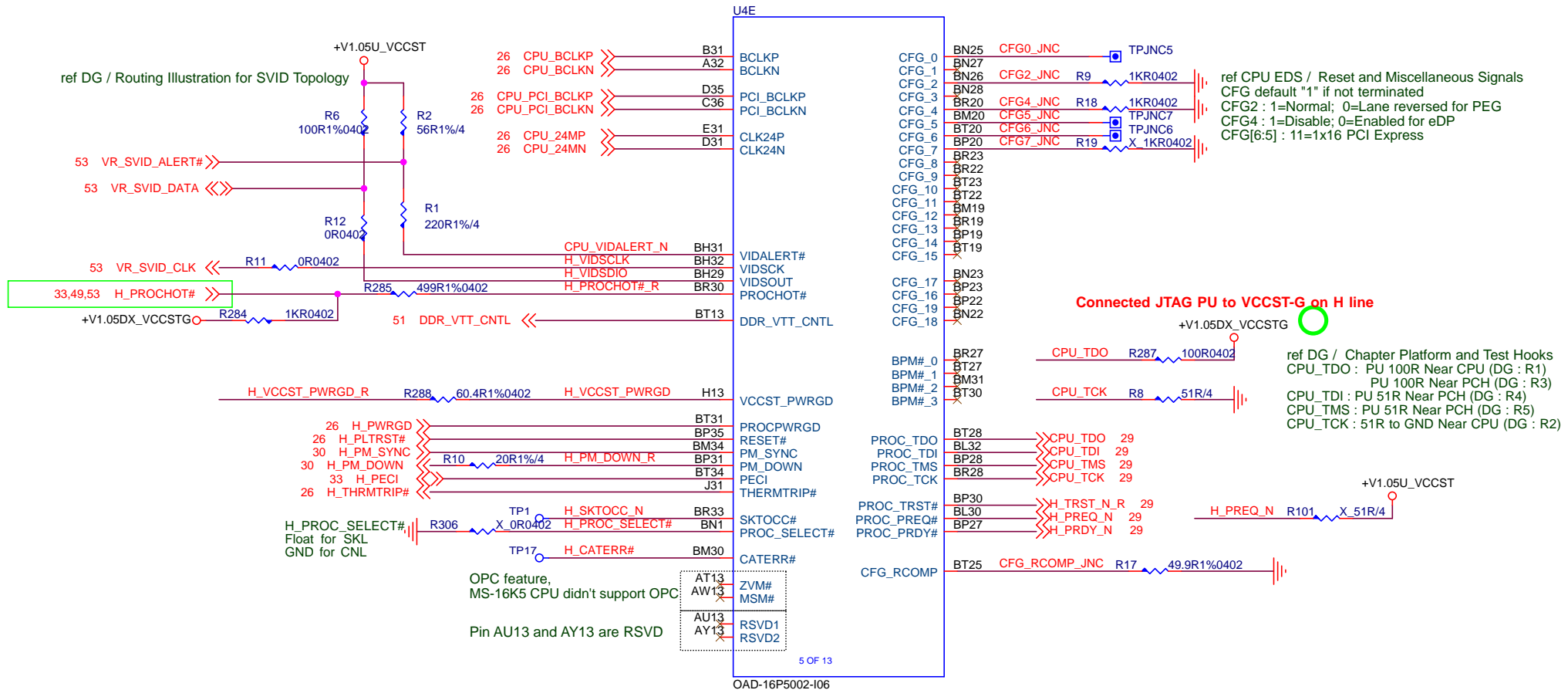
Intel Coffee Lake-H



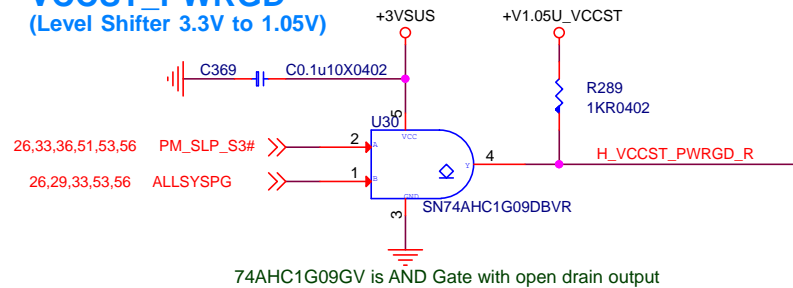
ref DG Chapter45 Power Sequencing Spec



CFL-H (HOST)



VCCST_PWRGD
(Level Shifter 3.3V to 1.05V)



DDR Channel A

9 M_A_DQ[63:0] <<>	U4A	DDR0_DQ_0/DDR0_DQ_0	DDR0_CK_0/DDR0_CK_0	AG1	M_A_CLK_DDRP0 9
M_A_DQ01	BR6	DDR0_DQ_1/DDR0_DQ_1	DDR0_CK_1/DDR0_CK_1	AG2	M_A_CLK_DDRN0 9
M_A_DQ02	BP6	DDR0_DQ_2/DDR0_DQ_2	DDR0_CK_2/DDR0_CK_2	AK2	M_A_CLK_DDRP1 9
M_A_DQ03	BR3	DDR0_DQ_3/DDR0_DQ_3	DDR0_CK_3/DDR0_CK_3	AK1	M_A_CLK_DDRN1 9
M_A_DQ04	BN5	DDR0_DQ_4/DDR0_DQ_4	NC/DDR0_CK_0	AL3	
M_A_DQ05	BP6	DDR0_DQ_5/DDR0_DQ_5	NC/DDR0_CK_1	AK3	
M_A_DQ06	BP2	DDR0_DQ_6/DDR0_DQ_6	NC/DDR0_CK_2	AL2	
M_A_DQ07	BN3	DDR0_DQ_7/DDR0_DQ_7	NC/DDR0_CK_3	AL1	
M_A_DQ08	BL4	DDR0_DQ_8/DDR0_DQ_8	DDR0_CKE_0/DDR0_CKE_0	AT1	M_A_CKE0 9
M_A_DQ09	BL5	DDR0_DQ_9/DDR0_DQ_9	DDR0_CKE_1/DDR0_CKE_1	AT2	M_A_CKE1 9
M_A_DQ10	BM1	DDR0_DQ_10/DDR0_DQ_10	DDR0_CKE_2/DDR0_CKE_2	AT3	
M_A_DQ11	BL2	DDR0_DQ_11/DDR0_DQ_11	DDR0_CKE_3/DDR0_CKE_3	AT5	
M_A_DQ12	BK4	DDR0_DQ_12/DDR0_DQ_12	DDR0_CS#_0/DDR0_CS#_0	AD5	M_A_CSNO 9
M_A_DQ13	BK5	DDR0_DQ_13/DDR0_DQ_13	DDR0_CS#_1/DDR0_CS#_1	AD2	M_A_CSNI 9
M_A_DQ14	BK1	DDR0_DQ_14/DDR0_DQ_14	NC/DDR0_CS#_2	AE5	
M_A_DQ15	BK2	DDR0_DQ_15/DDR0_DQ_15	NC/DDR0_CS#_3	AD3	
M_A_DQ16	BG4	DDR0_DQ_16/DDR0_DQ_16	DDR0_ODT_0/DDR0_ODT_0	AE4	M_A_ODT0 9
M_A_DQ17	BG5	DDR0_DQ_17/DDR0_DQ_17	NC/DDR0_ODT_1	AE1	M_A_ODT1 9
M_A_DQ18	BF4	DDR0_DQ_18/DDR0_DQ_18	NC/DDR0_ODT_2	AD4	
M_A_DQ19	BF5	DDR0_DQ_19/DDR0_DQ_19	NC/DDR0_ODT_3	AH5	M_A_BA0 9
M_A_DQ20	BG2	DDR0_DQ_20/DDR0_DQ_20	DDR0_CAB_4/DDR0_CAB_4	AH1	M_A_BA1 9
M_A_DQ21	BG1	DDR0_DQ_21/DDR0_DQ_21	DDR0_CAB_5/DDR0_CAB_5	AUT	M_A_BG0 9
M_A_DQ22	BF1	DDR0_DQ_22/DDR0_DQ_22	DDR0_CAB_6/DDR0_CAB_6	AH4	M_A_A16_RASN 9
M_A_DQ23	BF2	DDR0_DQ_23/DDR0_DQ_23	DDR0_CAB_7/DDR0_CAB_7	AG1	M_A_A14_WEN 9
M_A_DQ24	BD2	DDR0_DQ_24/DDR0_DQ_24	DDR0_CAB_8/DDR0_CAB_8	AH3	M_A_A0 9
M_A_DQ25	BD1	DDR0_DQ_25/DDR0_DQ_25	DDR0_CAB_9/DDR0_CAB_9	AP4	M_A_A1 9
M_A_DQ26	BC4	DDR0_DQ_26/DDR0_DQ_26	DDR0_CAB_10/DDR0_CAB_10	AN4	M_A_A2 9
M_A_DQ27	BC5	DDR0_DQ_27/DDR0_DQ_27	DDR0_CAB_11/DDR0_CAB_11	AP5	M_A_A3 9
M_A_DQ28	BD5	DDR0_DQ_28/DDR0_DQ_28	DDR0_CAB_12/DDR0_CAB_12	AP2	M_A_A4 9
M_A_DQ29	BD4	DDR0_DQ_29/DDR0_DQ_29	DDR0_CAB_13/DDR0_CAB_13	AP1	M_A_A5 9
M_A_DQ30	BC1	DDR0_DQ_30/DDR0_DQ_30	DDR0_CAB_14/DDR0_CAB_14	AP3	M_A_A6 9
M_A_DQ31	BC2	DDR0_DQ_31/DDR0_DQ_31	DDR0_CAB_15/DDR0_CAB_15	AN1	M_A_A7 9
M_A_DQ32	AB1	DDR0_DQ_32/DDR0_DQ_32	DDR0_CAB_16/DDR0_CAB_16	AN3	M_A_A8 9
M_A_DQ33	AB2	DDR0_DQ_33/DDR0_DQ_33	DDR0_CAB_17/DDR0_CAB_17	AT4	M_A_A9 9
M_A_DQ34	AA4	DDR0_DQ_34/DDR0_DQ_34	DDR0_CAB_18/DDR0_CAB_18	AH2	M_A_A10 9
M_A_DQ35	AA5	DDR0_DQ_35/DDR0_DQ_35	DDR0_CAB_19/DDR0_CAB_19	AN2	M_A_A11 9
M_A_DQ36	AB5	DDR0_DQ_36/DDR0_DQ_36	DDR0_CAB_20/DDR0_CAB_20	AU4	M_A_A12 9
M_A_DQ37	AB4	DDR0_DQ_37/DDR0_DQ_37	DDR0_CAB_21/DDR0_CAB_21	AE3	M_A_A13 9
M_A_DQ38	AA2	DDR0_DQ_38/DDR0_DQ_38	DDR0_CAB_22/DDR0_CAB_22	AU2	M_A_BG1 9
M_A_DQ39	AA1	DDR0_DQ_39/DDR0_DQ_39	DDR0_CAB_23/DDR0_CAB_23	AU3	M_A_ACTN 9
M_A_DQ40	V5	DDR0_DQ_40/DDR0_DQ_40	DDR0_CAB_24/DDR0_CAB_24	AG3	DDR0_A_PARITY 9
M_A_DQ41	V2	DDR0_DQ_41/DDR0_DQ_41	DDR0_CAB_25/DDR0_CAB_25	AU5	DDR0_A_ALERTN 9
M_A_DQ42	U1	DDR0_DQ_42/DDR0_DQ_42	DDR0_CAB_26/DDR0_CAB_26	BR5	M_A_DQSN0 9
M_A_DQ43	U2	DDR0_DQ_43/DDR0_DQ_43	DDR0_CAB_27/DDR0_CAB_27	BL3	M_A_DQSN1 9
M_A_DQ44	U1	DDR0_DQ_44/DDR0_DQ_44	DDR0_CAB_28/DDR0_CAB_28	BG3	M_A_DQSN2 9
M_A_DQ45	U5	DDR0_DQ_45/DDR0_DQ_45	DDR0_CAB_29/DDR0_CAB_29	B03	M_A_DQSN3 9
M_A_DQ46	U6	DDR0_DQ_46/DDR0_DQ_46	DDR0_CAB_30/DDR0_CAB_30	AA3	M_A_DQSN4 9
M_A_DQ47	U4	DDR0_DQ_47/DDR0_DQ_47	DDR0_CAB_31/DDR0_CAB_31	U3	M_A_DQSN5 9
M_A_DQ48	R2	DDR0_DQ_48/DDR0_DQ_48	DDR0_CAB_32/DDR0_CAB_32	P3	M_A_DQSN6 9
M_A_DQ49	P5	DDR0_DQ_49/DDR0_DQ_49	DDR0_CAB_33/DDR0_CAB_33	L3	M_A_DQSN7 9
M_A_DQ50	R4	DDR0_DQ_50/DDR0_DQ_50	DDR0_CAB_34/DDR0_CAB_34	BP5	M_A_DQSP0 9
M_A_DQ51	P4	DDR0_DQ_51/DDR0_DQ_51	DDR0_CAB_35/DDR0_CAB_35	BK3	M_A_DQSP1 9
M_A_DQ52	R5	DDR0_DQ_52/DDR0_DQ_52	DDR0_CAB_36/DDR0_CAB_36	BF3	M_A_DQSP2 9
M_A_DQ53	P2	DDR0_DQ_53/DDR0_DQ_53	DDR0_CAB_37/DDR0_CAB_37	BC3	M_A_DQSP3 9
M_A_DQ54	R1	DDR0_DQ_54/DDR0_DQ_54	DDR0_CAB_38/DDR0_CAB_38	AB3	M_A_DQSP4 9
M_A_DQ55	P1	DDR0_DQ_55/DDR0_DQ_55	DDR0_CAB_39/DDR0_CAB_39	V3	M_A_DQSP5 9
M_A_DQ56	M4	DDR0_DQ_56/DDR0_DQ_56	DDR0_CAB_40/DDR0_CAB_40	R3	M_A_DQSP6 9
M_A_DQ57	M1	DDR0_DQ_57/DDR0_DQ_57	DDR0_CAB_41/DDR0_CAB_41	M3	M_A_DQSP7 9
M_A_DQ58	L4	DDR0_DQ_58/DDR0_DQ_58	DDR0_CAB_42/DDR0_CAB_42	AY3	
M_A_DQ59	L2	DDR0_DQ_59/DDR0_DQ_59	DDR0_CAB_43/DDR0_CAB_43	BA3	
M_A_DQ60	M5	DDR0_DQ_60/DDR0_DQ_60	DDR0_CAB_44/DDR0_CAB_44		
M_A_DQ61	M2	DDR0_DQ_61/DDR0_DQ_61	DDR0_CAB_45/DDR0_CAB_45		
M_A_DQ62	L5	DDR0_DQ_62/DDR0_DQ_62	DDR0_CAB_46/DDR0_CAB_46		
M_A_DQ63	L1	DDR0_DQ_63/DDR0_DQ_63	DDR0_CAB_47/DDR0_CAB_47		
BA2	NC/DDR0_ECC_0	DDR0_DQSP_0/DDR0_DQSP_0	DDR0_DQSP_1/DDR0_DQSP_1		
AY3	NC/DDR0_ECC_1	DDR0_DQSP_2/DDR0_DQSP_2	DDR0_DQSP_3/DDR0_DQSP_3		
AY5	NC/DDR0_ECC_2	DDR0_DQSP_4/DDR0_DQSP_4	DDR0_DQSP_5/DDR0_DQSP_5		
BA5	NC/DDR0_ECC_3	DDR0_DQSP_6/DDR0_DQSP_6	DDR0_DQSP_7/DDR0_DQSP_7		
BA4	NC/DDR0_ECC_4	DDR0_DQSP_8/DDR0_DQSP_8	DDR0_DQSP_9/DDR0_DQSP_9		
AY7	NC/DDR0_ECC_5	DDR0_DQSP_10/DDR0_DQSP_10	DDR0_DQSP_11/DDR0_DQSP_11		
AY2	NC/DDR0_ECC_6	DDR0_DQSP_12/DDR0_DQSP_12	DDR0_DQSP_13/DDR0_DQSP_13		
AY2	NC/DDR0_ECC_7	DDR0_DQSP_14/DDR0_DQSP_14	DDR0_DQSP_15/DDR0_DQSP_15		

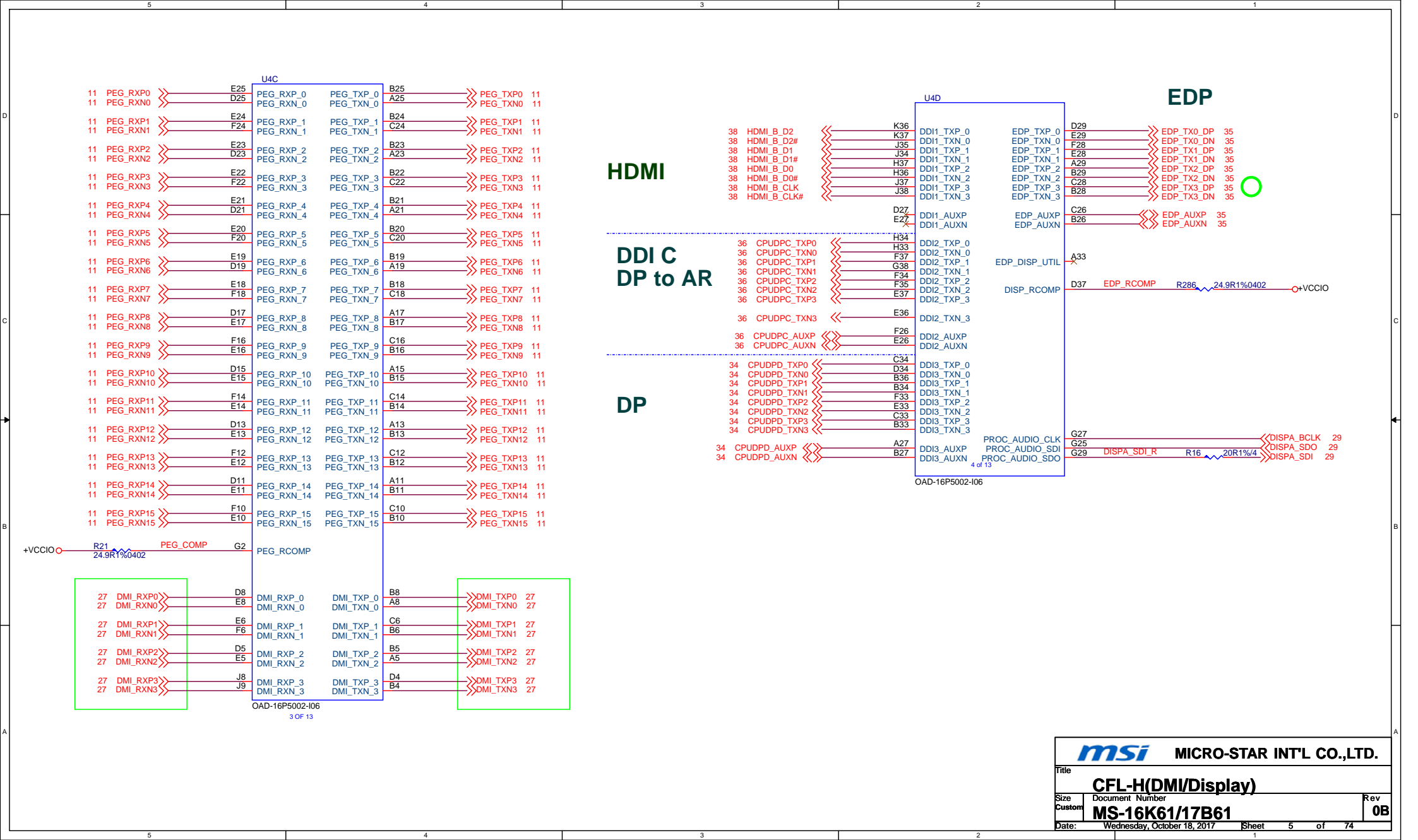
OAD-16P5002-106 DDR CHANNEL A

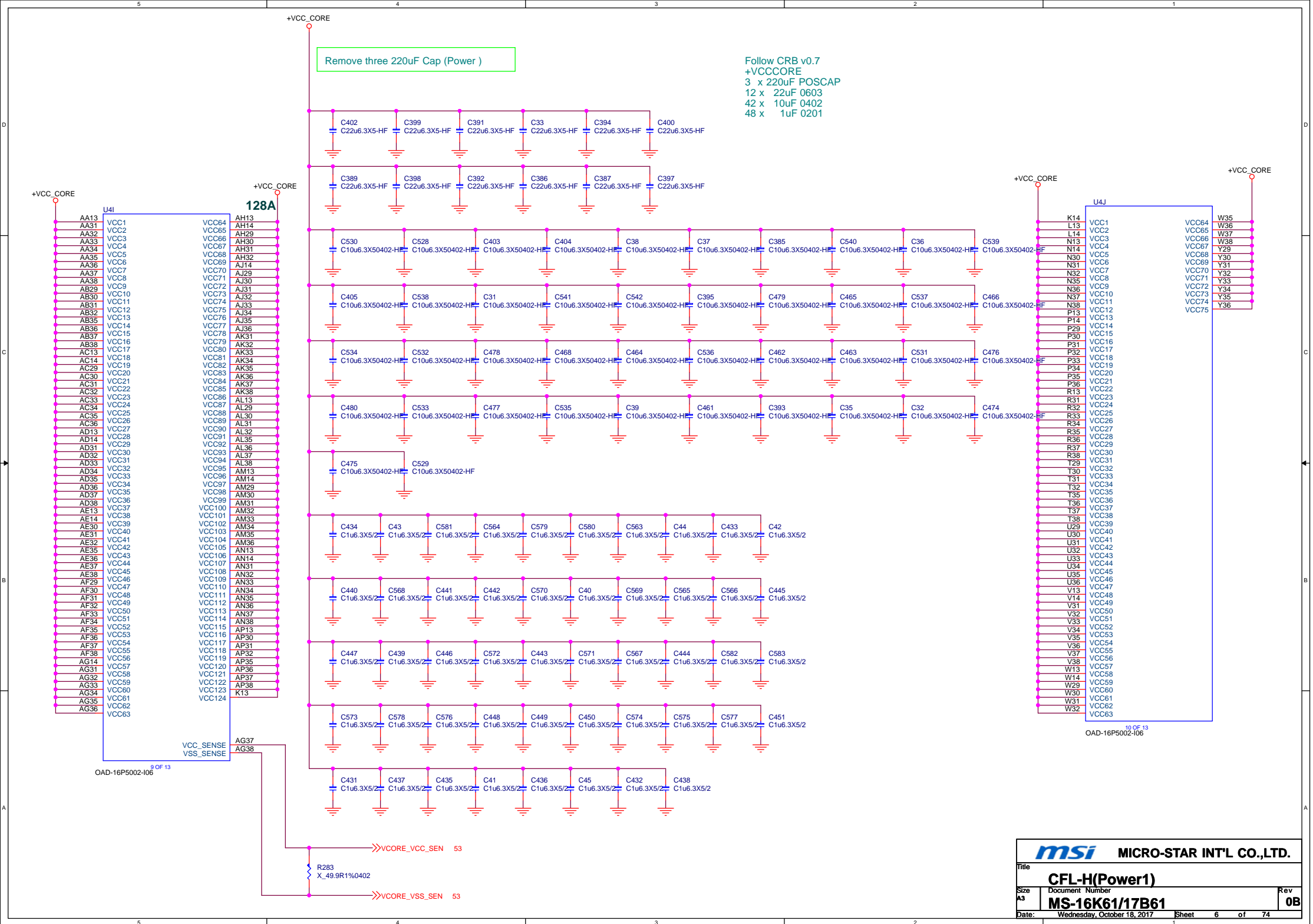
DDR Channel B

10 M_B_DQ[63:0] <<>	U4B	DDR1_DQ_0/DDR1_DQ_0	DDR1_CK_0/DDR1_CK_0	AM9	M_B_CLK_DDRP0 10
M_B_DQ01	BT11	DDR1_DQ_1/DDR1_DQ_1	DDR1_CK_1/DDR1_CK_1	AM9	M_B_CLK_DDRN0 10
M_B_DQ02	BT9	DDR1_DQ_2/DDR1_DQ_2	DDR1_CK_2/DDR1_CK_2	AM7	M_B_CLK_DDRP1 10
M_B_DQ03	BR8	DDR1_DQ_3/DDR1_DQ_3	DDR1_CK_3/DDR1_CK_3	AM8	M_B_CLK_DDRN1 10
M_B_DQ04	BP11	DDR1_DQ_4/DDR1_DQ_4	NC/DDR1_CK_0	AM11	
M_B_DQ05	BN11	DDR1_DQ_5/DDR1_DQ_5	NC/DDR1_CK_1	AM10	
M_B_DQ06	BP8	DDR1_DQ_6/DDR1_DQ_6	NC/DDR1_CK_2	AM10	
M_B_DQ07	BN8	DDR1_DQ_7/DDR1_DQ_7	NC/DDR1_CK_3	AM11	
M_B_DQ08	BL12	DDR1_DQ_8/DDR1_DQ_8	DDR1_CKE_0/DDR1_CKE_0	AT8	M_B_CKE0 10
M_B_DQ09	BL11	DDR1_DQ_9/DDR1_DQ_9	DDR1_CKE_1/DDR1_CKE_1	AT10	M_B_CKE1 10
M_B_DQ10	BL8	DDR1_DQ_10/DDR1_DQ_10	DDR1_CKE_2/DDR1_CKE_2	AT7	
M_B_DQ11	BJ8	DDR1_DQ_11/DDR1_DQ_11	DDR1_CKE_3/DDR1_CKE_3	AT11	
M_B_DQ12	BJ11	DDR1_DQ_12/DDR1_DQ_12	DDR1_CS#_0/DDR1_CS#_0	AF11	M_B_CSNO 10
M_B_DQ13	BJ10	DDR1_DQ_13/DDR1_DQ_13	DDR1_CS#_1/DDR1_CS#_1	AF10	M_B_CSNI 10
M_B_DQ14	BL7	DDR1_DQ_14/DDR1_DQ_14	NC/DDR1_CS#_2	AE10	
M_B_DQ15	BJ7	DDR1_DQ_15/DDR1_DQ_15	NC/DDR1_CS#_3	AF7	
M_B_DQ16	BG11	DDR1_DQ_16/DDR1_DQ_16	DDR1_ODT_0/DDR1_ODT_0	AE8	M_B_ODT0 10
M_B_DQ17	BG10	DDR1_DQ_17/DDR1_DQ_17	NC/DDR1_ODT_1	AE9	M_B_ODT1 10
M_B_DQ18	BG8	DDR1_DQ_18/DDR1_DQ_18	NC/DDR1_ODT_2	AE11	
M_B_DQ19	BF8	DDR1_DQ_19/DDR1_DQ_19	NC/DDR1_ODT_3	AH10	M_B_A16_RASN 10
M_B_DQ20	BF11	DDR1_DQ_20/DDR1_DQ_20	DDR1_CAB_3/DDR1_CAB_3	AH11	M_B_A15_WEN 10
M_B_DQ21	BF10	DDR1_DQ_21/DDR1_DQ_21	DDR1_CAB_4/DDR1_CAB_4	AF8	M_B_A15_CASN 10
M_B_DQ22	BG7	DDR1_DQ_22/DDR1_DQ_22	DDR1_CAB_5/DDR1_CAB_5	AH8	M_B_BA0 10
M_B_DQ23	BF7	DDR1_DQ_23/DDR1_DQ_23	DDR1_CAB_6/DDR1_CAB_6	AR9	M_B_BA1 10
M_B_DQ24	BB11	DDR1_DQ_24/DDR1_DQ_24	DDR1_CAB_7/DDR1_CAB_7	AR9	M_B_BG0 10
M_B_DQ25	BC11	DDR1_DQ_25/DDR1_DQ_25	DDR1_CAB_8/DDR1_CAB_8	AJ9	M_B_A0 10
M_B_DQ26	BB8	DDR1_DQ_26/DDR1_DQ_26	DDR1_CAB_9/DDR1_CAB_9	AK6	M_B_A1 10
M_B_DQ27	BC8	DDR1_DQ_27/DDR1_DQ_27	DDR1_CAB_10/DDR1_CAB_10	AK5	M_B_A2 10
M_B_DQ28	BC10	DDR1_DQ_28/DDR1_DQ_28	DDR1_CAB_11/DDR1_CAB_11	AL5	M_B_A3 10
M_B_DQ29	BB10	DDR1_DQ_29/DDR1_DQ_29	DDR1_CAB_12/DDR1_CAB_12	AL6	M_B_A4 10
M_B_DQ30	BC7	DDR1_DQ_30/DDR1_DQ_30	DDR1_CAB_13/DDR1_CAB_13	AM6	M_B_A5 10
M_B_DQ31	BB7	DDR1_DQ_31/DDR1_DQ_31	DDR1_CAB_14/DDR1_CAB_14	AN7	M_B_A6 10
M_B_DQ32	AA11	DDR1_DQ_32/DDR1_DQ_32	DDR1_CAB_15/DDR1_CAB_15	AN10	M_B_A7 10
M_B_DQ33	AA10	DDR1_DQ_33/DDR1_DQ_33	DDR1_CAB_16/DDR1_CAB_16	AN8	M_B_A8 10
M_B_DQ34	AC11	DDR1_DQ_34/DDR1_DQ_34	DDR1_CAB_17/DDR1_CAB_17	AR11	M_B_A9 10
M_B_DQ35	AC10	DDR1_DQ_35/DDR1_DQ_35	DDR1_CAB_18/DDR1_CAB_18	AH7	M_B_A10 10
M_B_DQ36	AA7	DDR1_DQ_36/DDR1_DQ_36	DDR1_CAB_19/DDR1_CAB_19	AN11	M_B_A11 10
M_B_DQ37	AA8	DDR1_DQ_37/DDR1_DQ_37	DDR1_CAB_20/DDR1_CAB_20	AR10	M_B_A12 10
M_B_DQ38	AC8	DDR1_DQ_38/DDR1_DQ_38	DDR1_CAB_21/DDR1_CAB_21	AF9	M_B_A13 10
M_B_DQ39	AC7	DDR1_DQ_39/DDR1_DQ_39	DDR1_CAB_22/DDR1_CAB_22	AR7	M_B_BG1 10
M_B_DQ40	W8	DDR1_DQ_40/DDR1_DQ_40	DDR1_CAB_23/DDR1_CAB_23	AT9	M_B_ACTN 10
M_B_DQ41	W7	DDR1_DQ_41/DDR1_DQ_41	DDR1_CAB_24/DDR1_CAB_24	AJ7	DDR1_B_PARITY 10
M_B_DQ42	V10	DDR1_DQ_42/DDR1_DQ_42	DDR1_CAB_25/DDR1_CAB_25	AR8	DDR1_B_ALERTN 10
M_B_DQ43	V11	DDR1_DQ_43/DDR1_DQ_43	DDR1_CAB_26/DDR1_CAB_26		
M_B_DQ44	W11	DDR1_DQ_44/DDR1_DQ_44	DDR1_CAB_27/DDR1_CAB_27		
M_B_DQ45	W10	DDR1_DQ_45/DDR1_DQ_45	DDR1_CAB_28/DDR1_CAB_28		
M_B_DQ46	V7	DDR1_DQ_46/DDR1_DQ_46	DDR1_CAB_29/DDR1_CAB_29		
M_B_DQ47	V8	DDR1_DQ_47/DDR1_DQ_47	DDR1_CAB_30/DDR1_CAB_30		
M_B_DQ48	R11	DDR1_DQ_48/DDR1_DQ_48	DDR1_CAB_31/DDR1_CAB_31		
M_B_DQ49	P11	DDR1_DQ_49/DDR1_DQ_49	DDR1_CAB_32/DDR1_CAB_32		
M_B_DQ50	P7	DDR1_DQ_50/DDR1_DQ_50	DDR1_CAB_33/DDR1_CAB_33		
M_B_DQ51	R8	DDR1_DQ_51/DDR1_DQ_51	DDR1_CAB_34/DDR1_CAB_34		
M_B_DQ52	R10	DDR1_DQ_52/DDR1_DQ_52	DDR1_CAB_35/DDR1_CAB_35		
M_B_DQ53	P10	DDR1_DQ_53/DDR1_DQ_53	DDR1_CAB_36/DDR1_CAB_36		
M_B_DQ54	R7	DDR1_DQ_54/DDR1_DQ_54	DDR1_CAB_37/DDR1_CAB_37		
M_B_DQ55	P8	DDR1_DQ_55/DDR1_DQ_55	DDR1_CAB_38/DDR1_CAB_38		
M_B_DQ56	L11	DDR1_DQ_56/DDR1_DQ_56	DDR1_CAB_39/DDR1_CAB_39		
M_B_DQ57	M11	DDR1_DQ_57/DDR1_DQ_57	DDR1_CAB_40/DDR1_CAB_40		
M_B_DQ58	L7	DDR1_DQ_58/DDR1_DQ_58	DDR1_CAB_41/DDR1_CAB_41		
M_B_DQ59	M8	DDR1_DQ_59/DDR1_DQ_59	DDR1_CAB_42/DDR1_CAB_42		
M_B_DQ60	L10	DDR1_DQ_60/DDR1_DQ_60	DDR1_CAB_43/DDR1_CAB_43		
M_B_DQ61	M10	DDR1_DQ_61/DDR1_DQ_61	DDR1_CAB_44/DDR1_CAB_44		
M_B_DQ62	M7	DDR1_DQ_62/DDR1_DQ_62	DDR1_CAB_45/DDR1_CAB_45		
M_B_DQ63	L8	DDR1_DQ_63/DDR1_DQ_63	DDR1_CAB_46/DDR1_CAB_46		
AW11	NC/DDR1_ECC_0	DDR1_DQSP_0/DDR1_DQSP_0	DDR1_DQSP_1/DDR1_DQSP_1		
AY10	NC/DDR1_ECC_1	DDR1_DQSP_2/DDR1_DQSP_2	DDR1_DQSP_3/DDR1_DQSP_3		
AY5	NC/DDR1_ECC_2	DDR1_DQSP_4/DDR1_DQSP_4	DDR1_DQSP_5/DDR1_DQSP_5		
AW8	NC/DDR1_ECC_3	DDR1_DQSP_6/DDR1_DQSP_6	DDR1_DQSP_7/DDR1_DQSP_7		
AY10	NC/DDR1_ECC_4	DDR1_DQSP_8/DDR1_DQSP_8	DDR1_DQSP_9/DDR1_DQSP_9		
AW10	NC/DDR1_ECC_5	DDR1_DQSP_10/DDR1_DQSP_10	DDR1_DQSP_11/DDR1_DQSP_11		
AY2	NC/DDR1_ECC_6	DDR1_DQSP_12/DDR1_DQSP_12	DDR1_DQSP_13/DDR1_DQSP_13		
AW7	NC/DDR1_ECC_7	DDR1_DQSP_14/DDR1_DQSP_14	DDR1_DQSP_15/DDR1_DQSP_15		

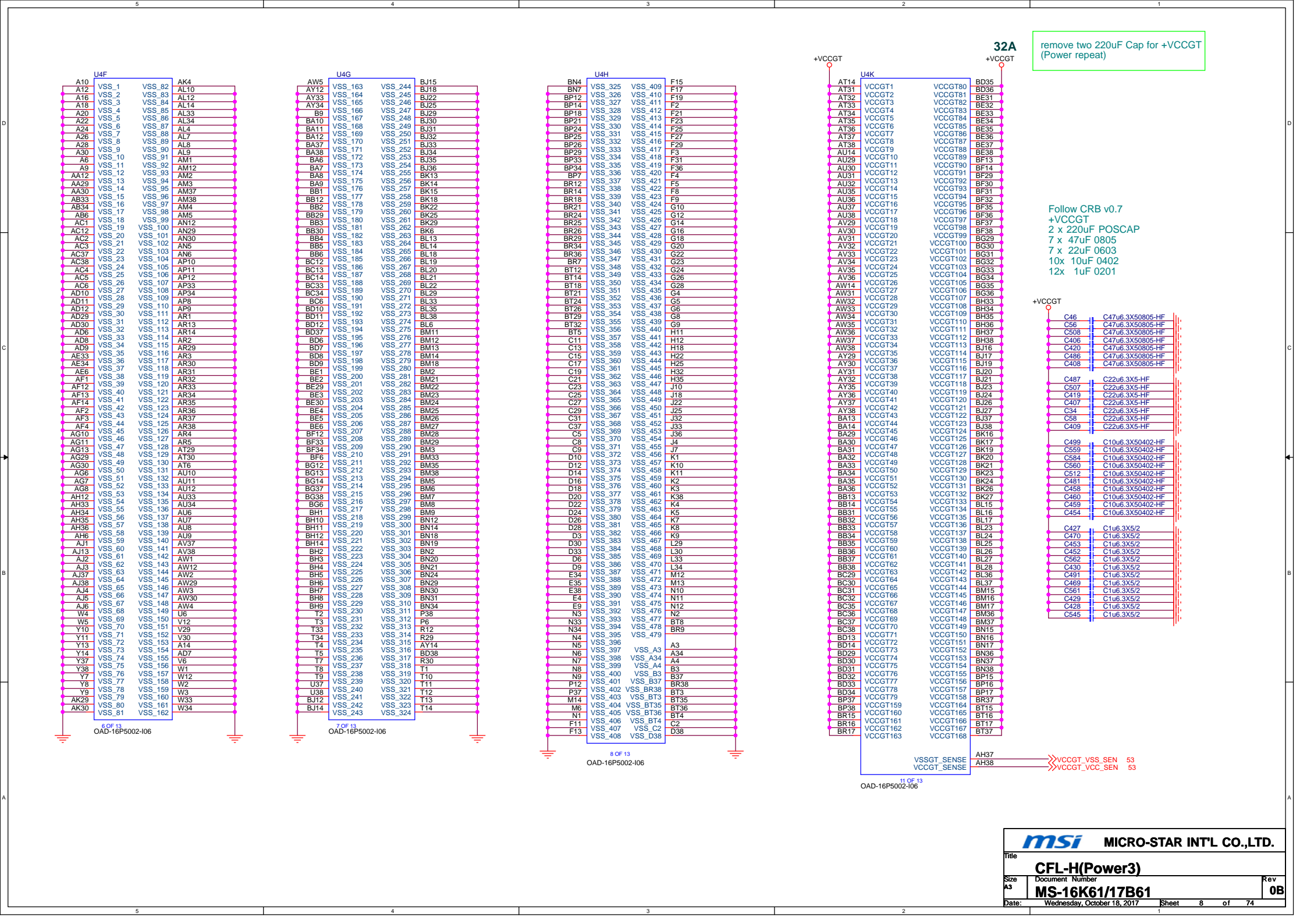
OAD-16P5002-106 DDR CHANNEL B

R308	121R1%0402	DDR_COMP0	G1	DDR_RCOMP_0	DDR_VREF_CA 9
R309	75R1%0402	DDR_COMP1	H1	DDR_RCOMP_1	DDR_VREF_CA 9
R310	100R1%0402	DDR_COMP2	J2	DDR_RCOMP_2	DDR_VREF_CA 9







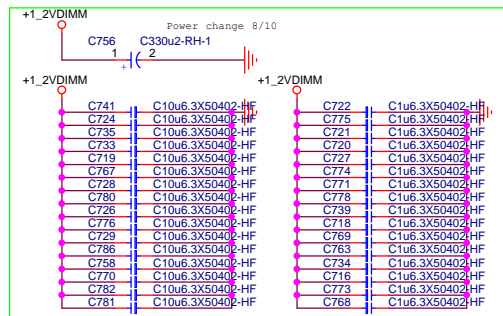


SODIMM_A0 (TOP-Reverse)

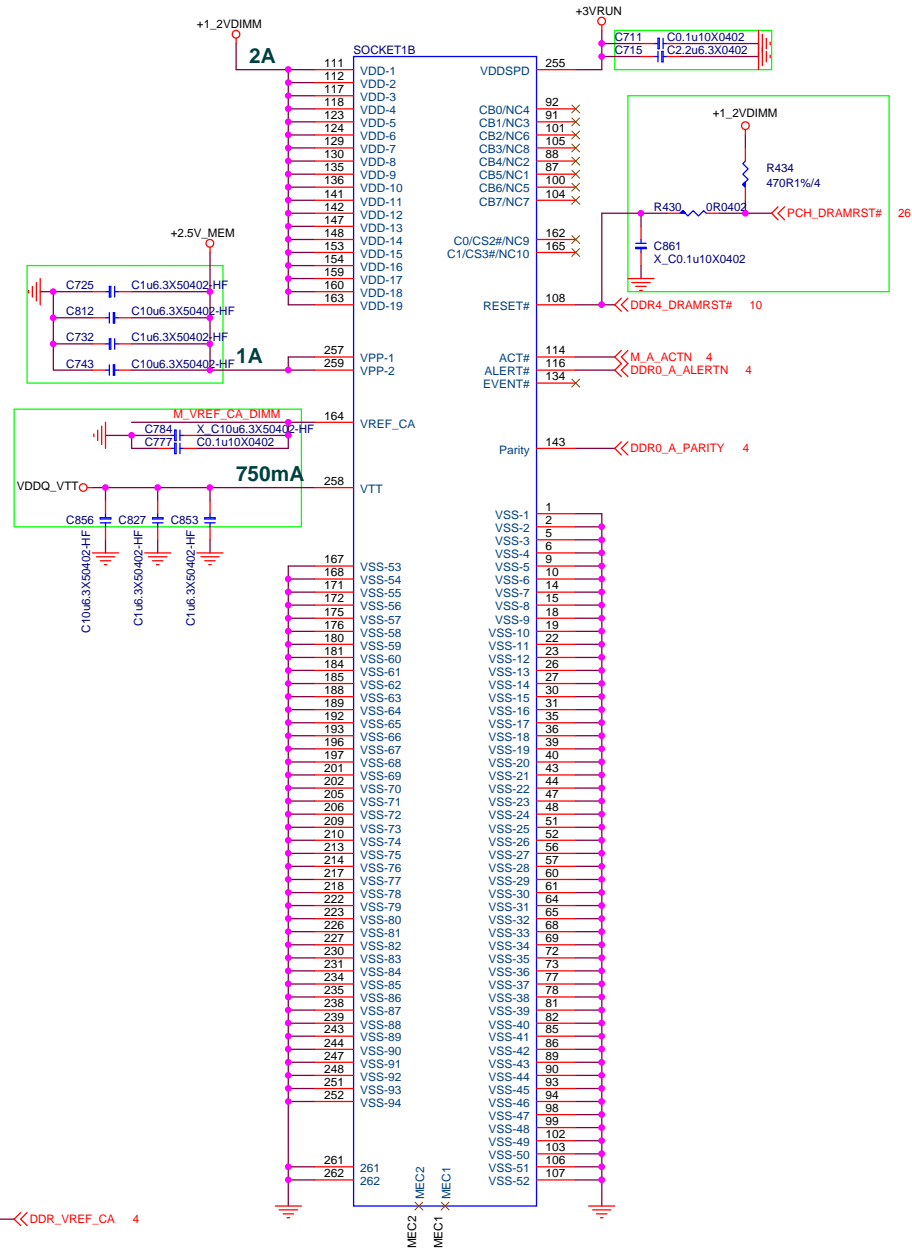


ref DG/ Section 4.14.1
CFL-H DDR4 SDDIMM Power Plane Decoupling

N13-2600220-L41



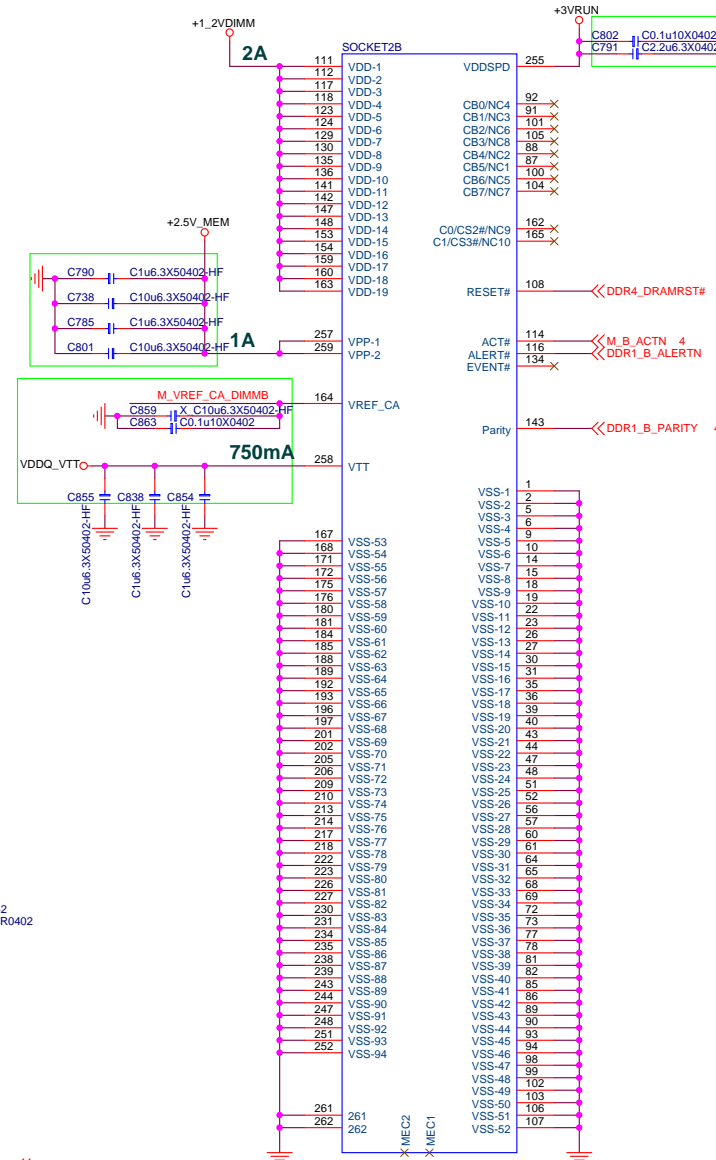
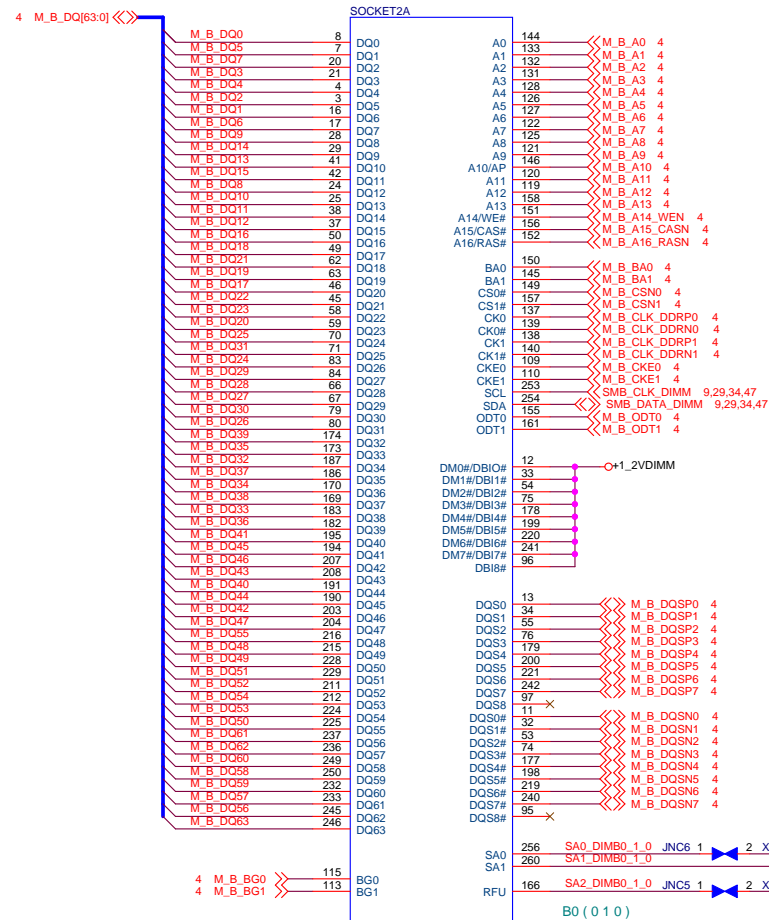
Vinafix.com



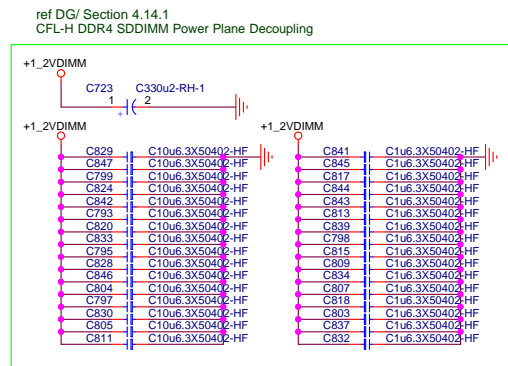
N13-2600220-L41

msi MICRO-STAR INT'L CO.,LTD.			
Title			
DDR4 SODIMM A0			
Size	Document	Number	Rev
Custom	MS-16K61/17B61		0B
Date:	Wednesday, October 18, 2017		
Sheet	9 of 74		

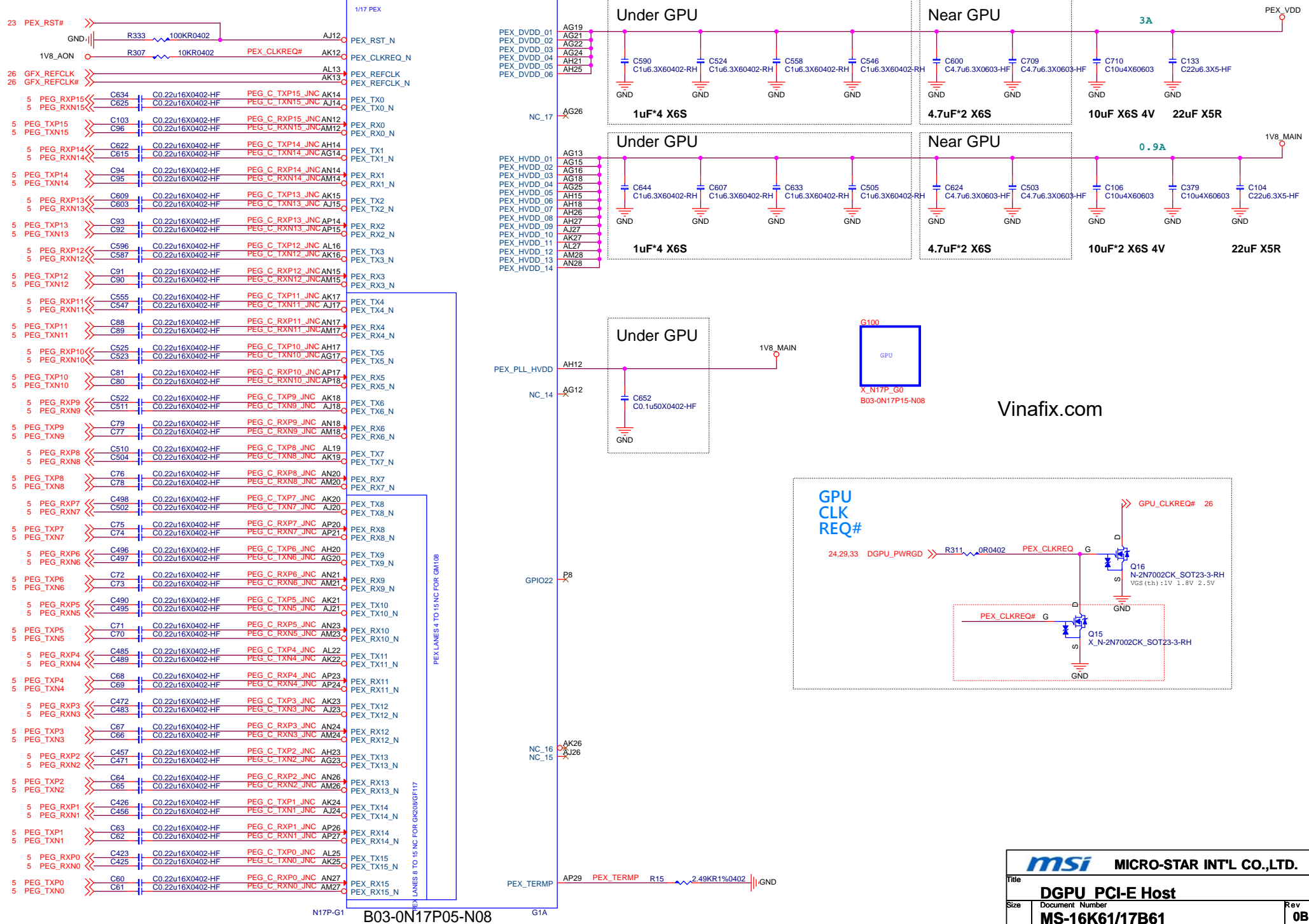
SODIMM_B0 (TOP-Standard)



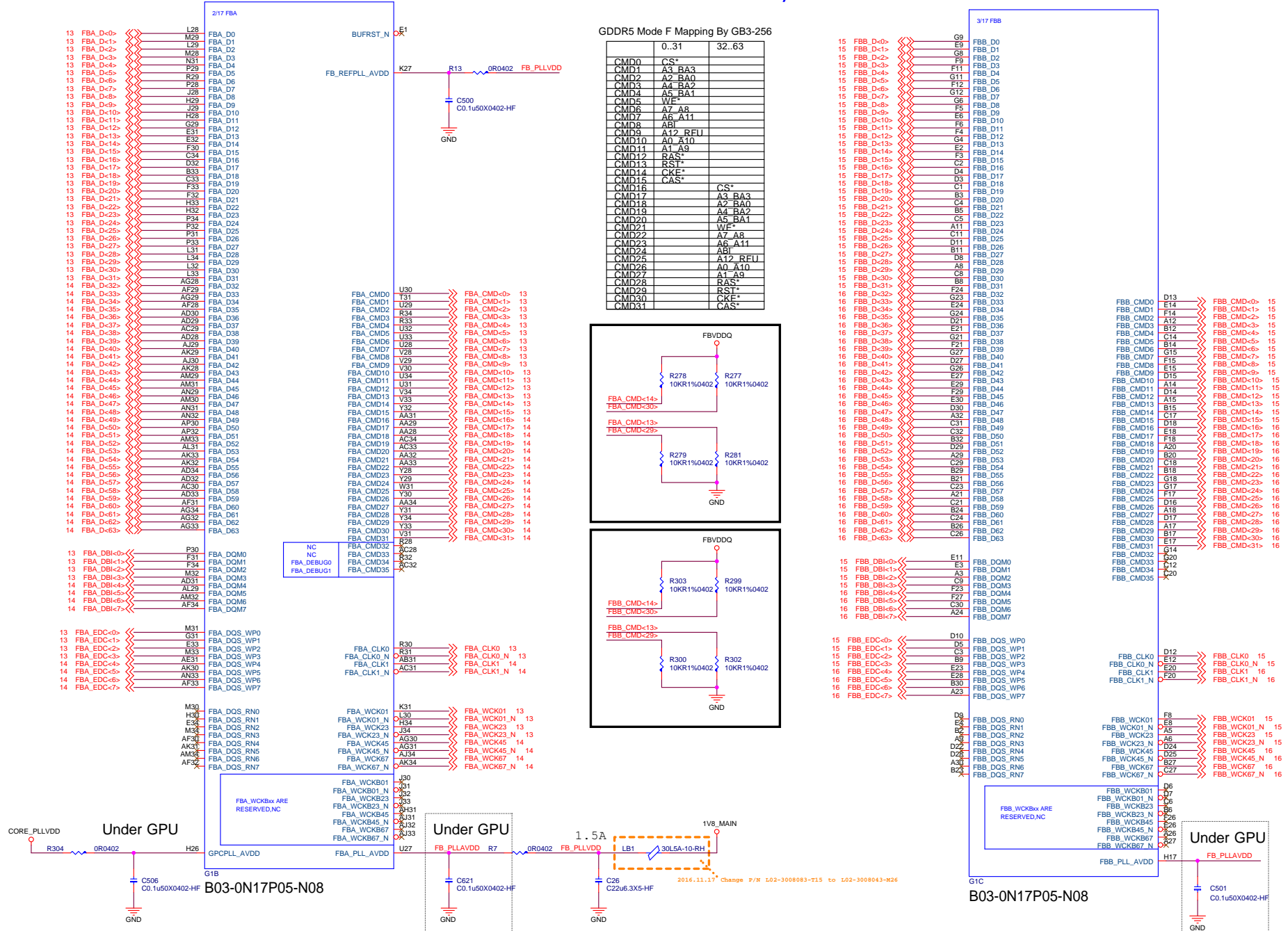
N13-2600230-L41



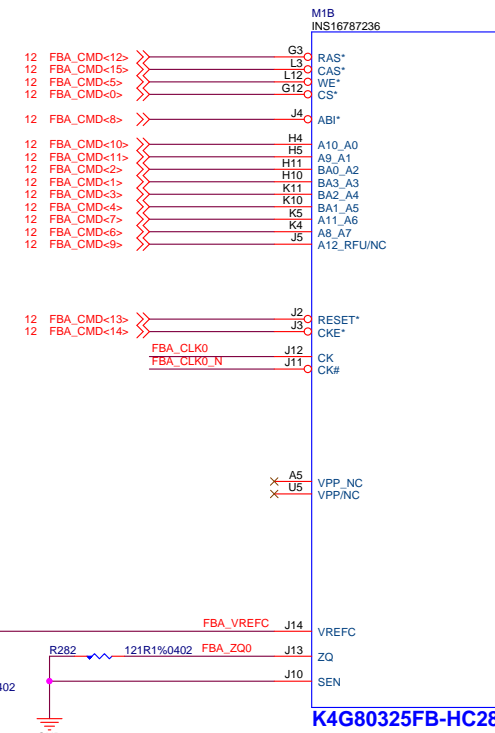
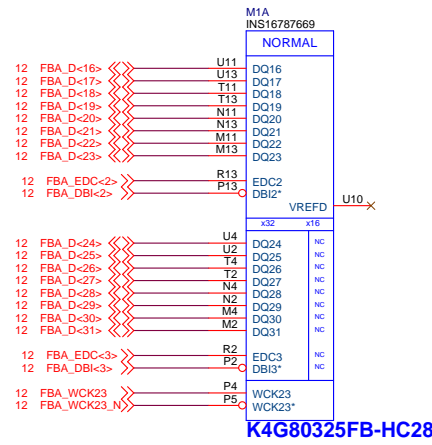
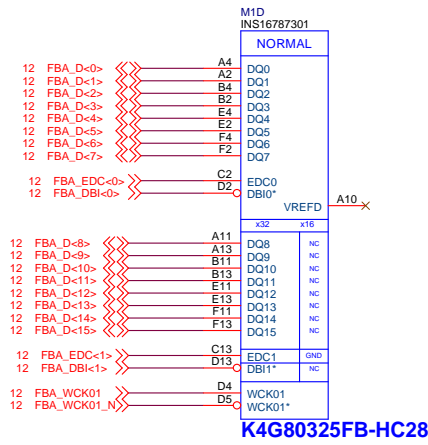
GPU PCI EXPRESS



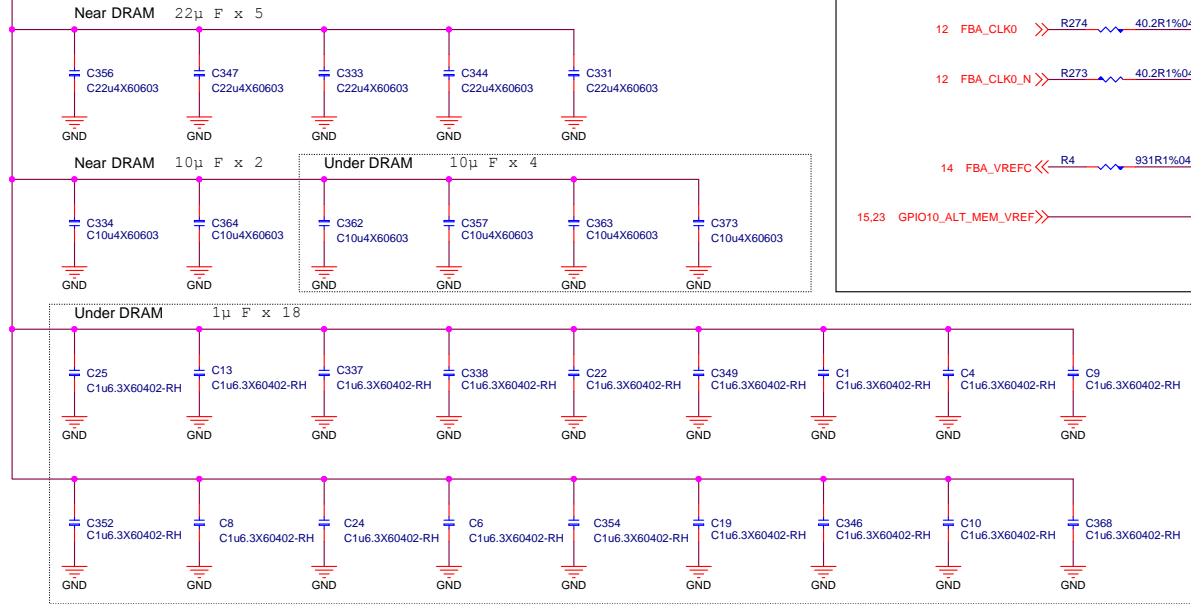
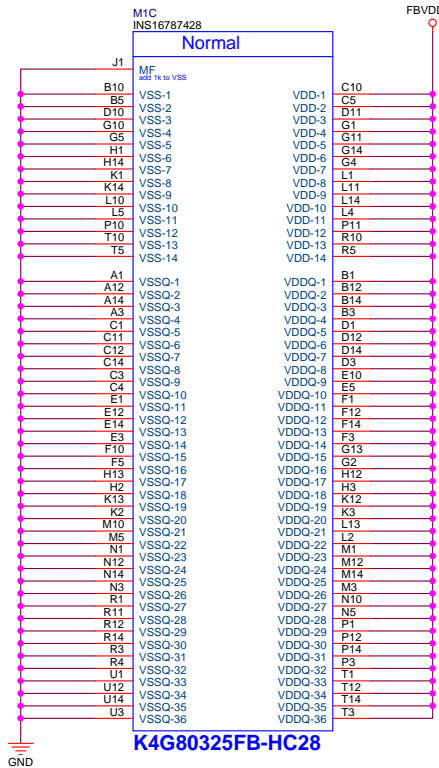
GPU Frame Buffer Partition A/B



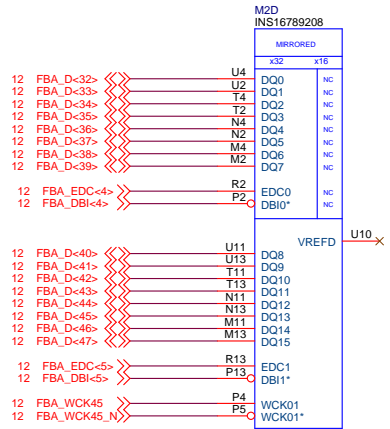
DGPU_GDDR5 FrameBuffer A0



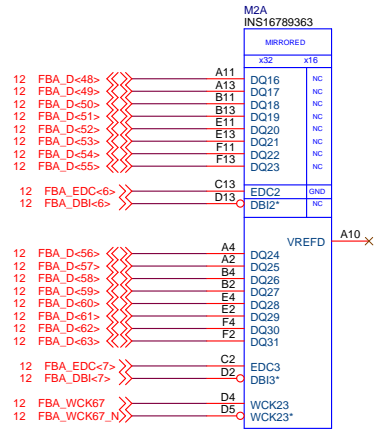
Vinafix.com



DGPU_GDDR5 FrameBuffer A1

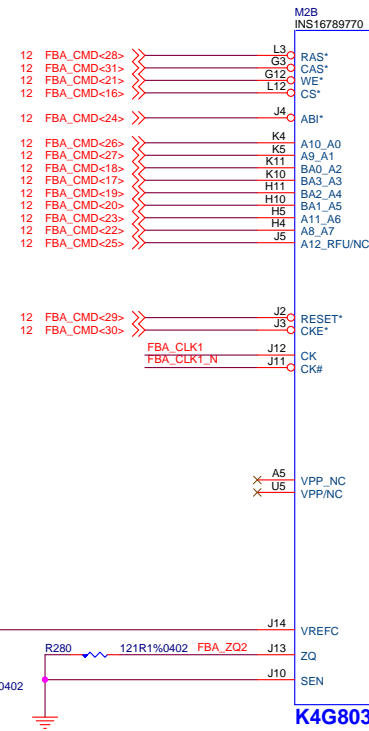


K4G80325FB-HC28

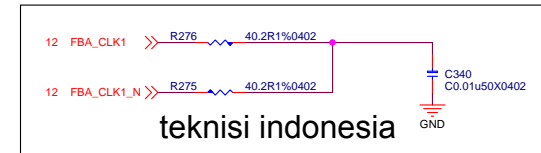
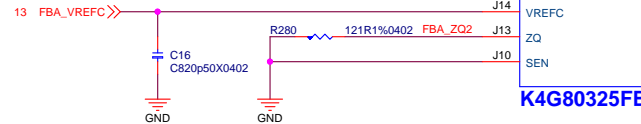


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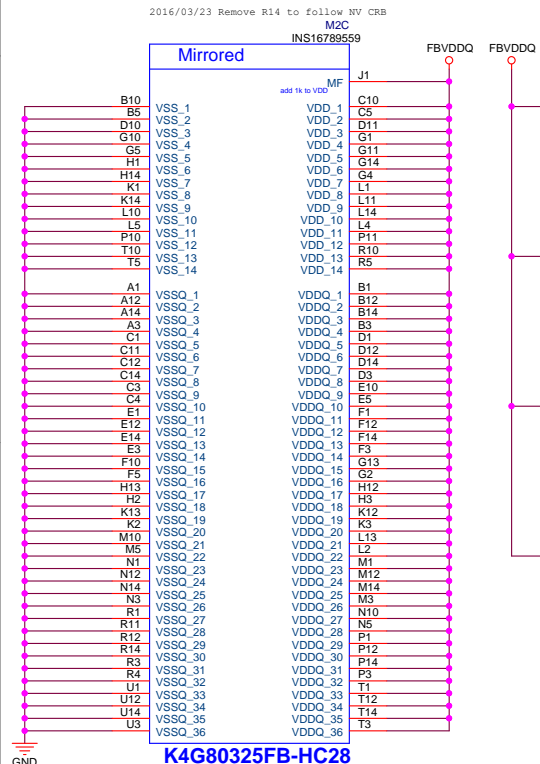
M12-8032545-S02



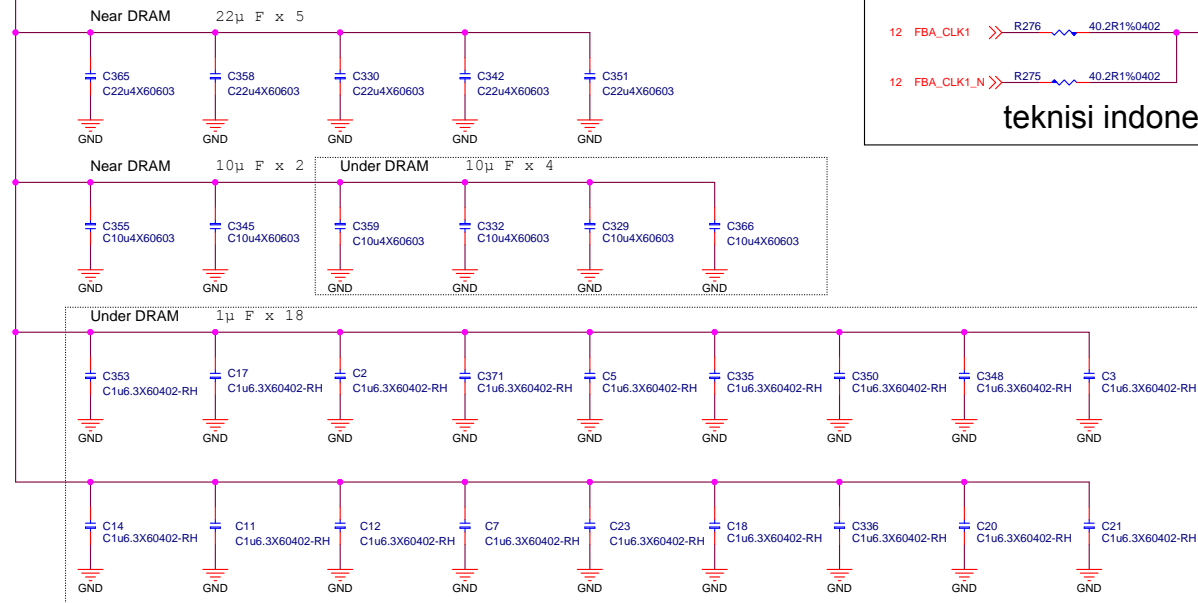
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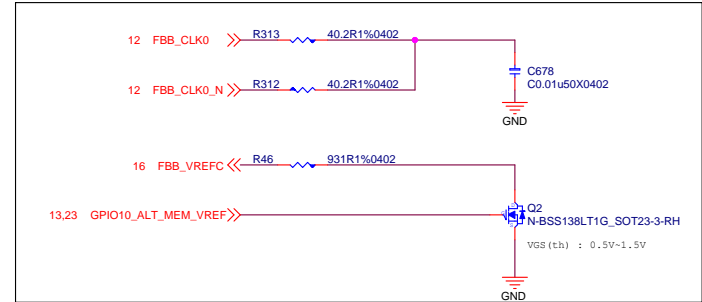
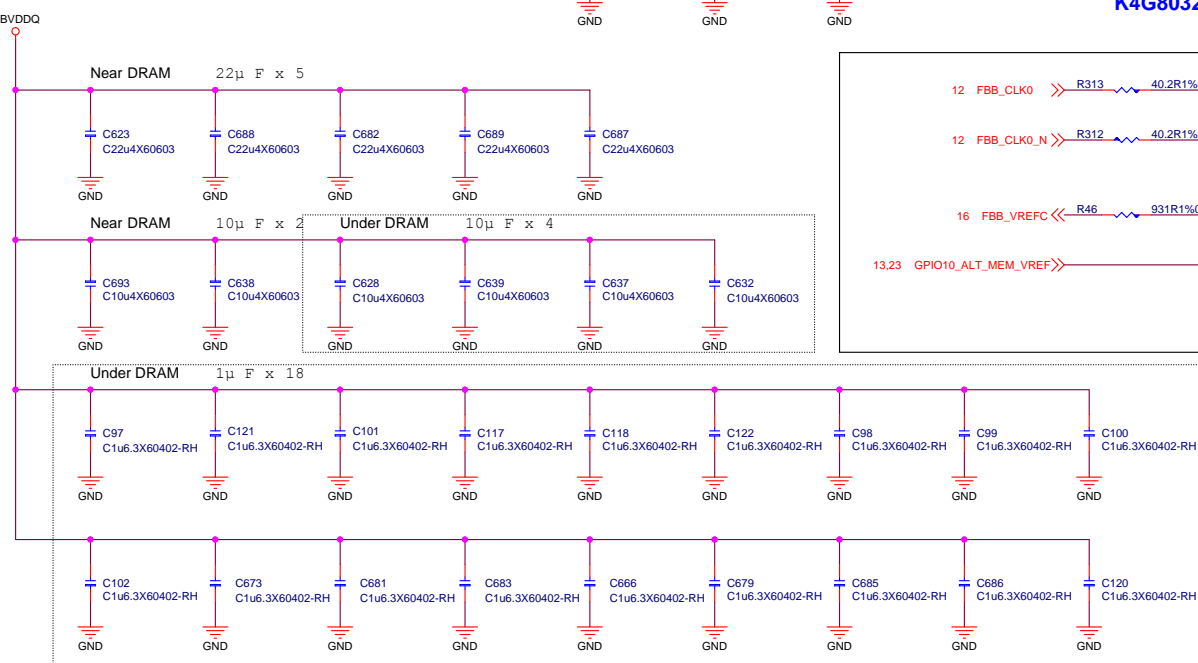
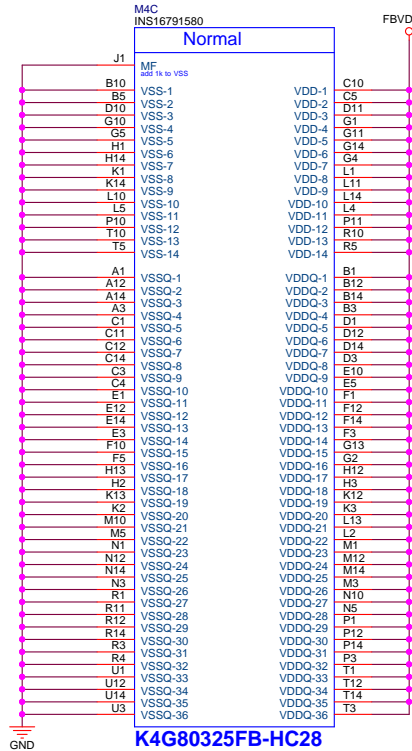
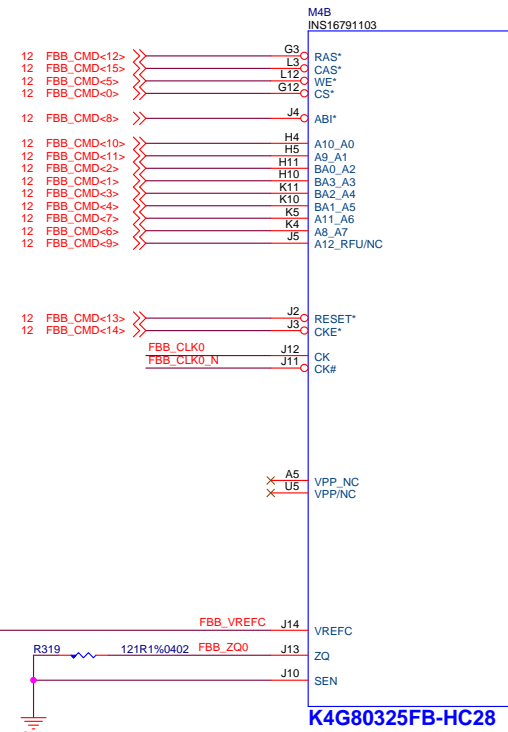
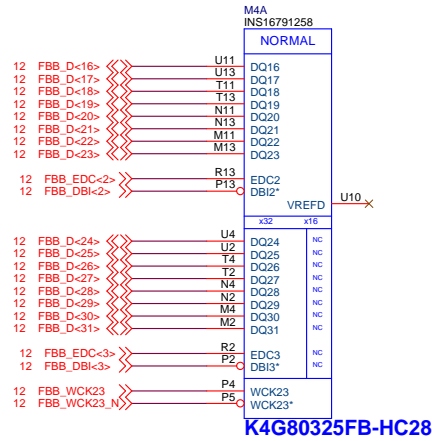
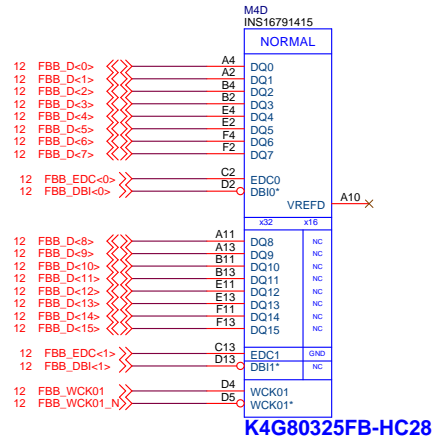
teknisi indonesia



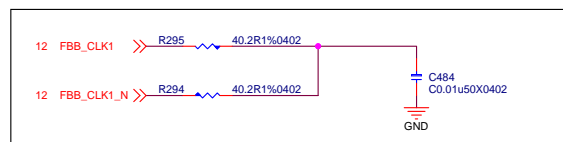
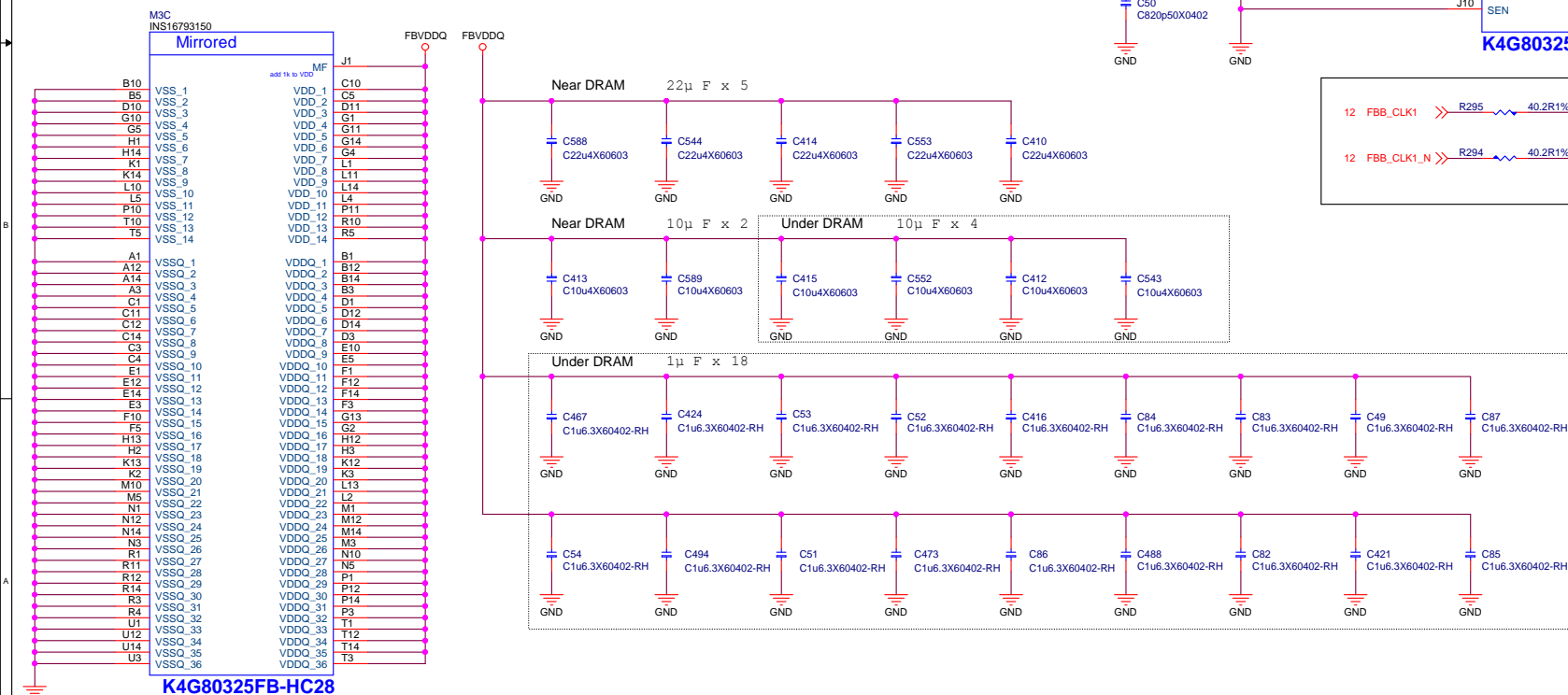
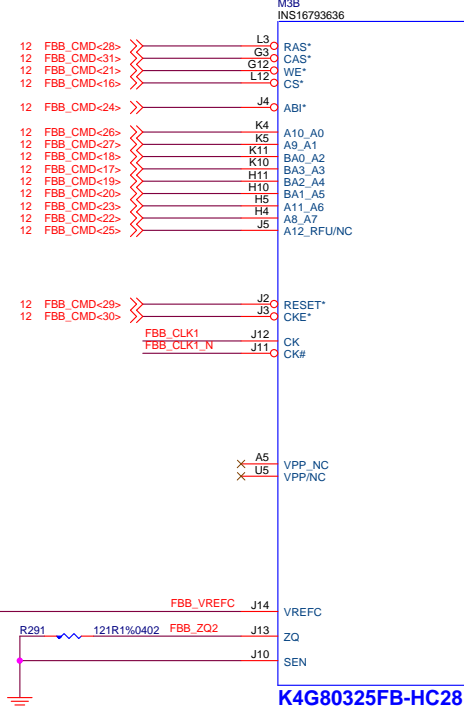
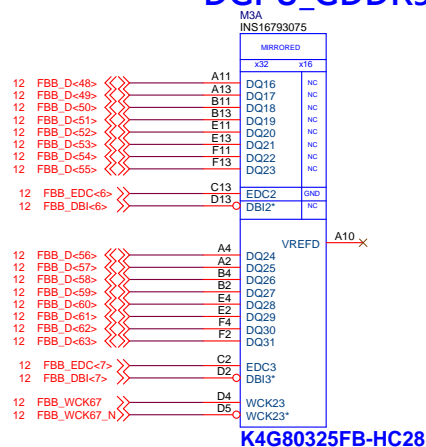
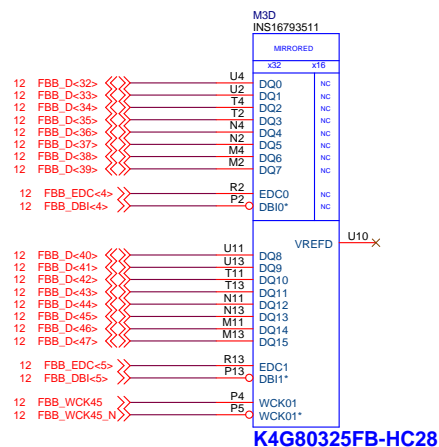
K4G80325FB-HC28



DGPU_GDDR5 FrameBuffer B0

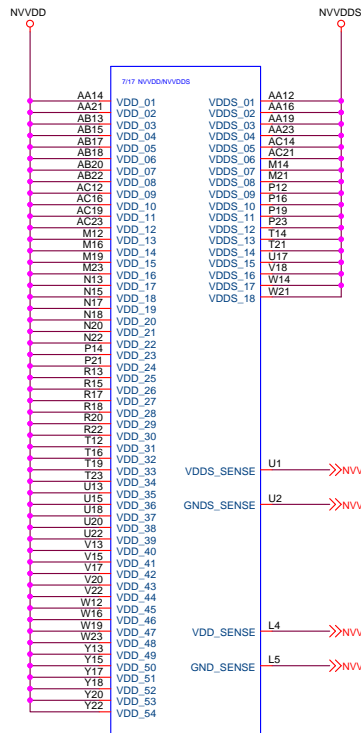


DGPU_GDDR5 FrameBuffer B1

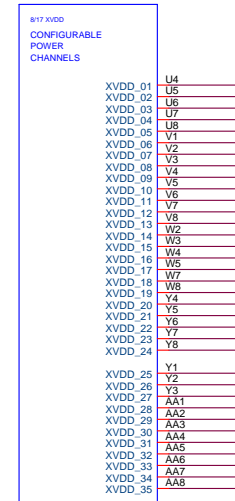


GPU NVVDD, FBVDDQ

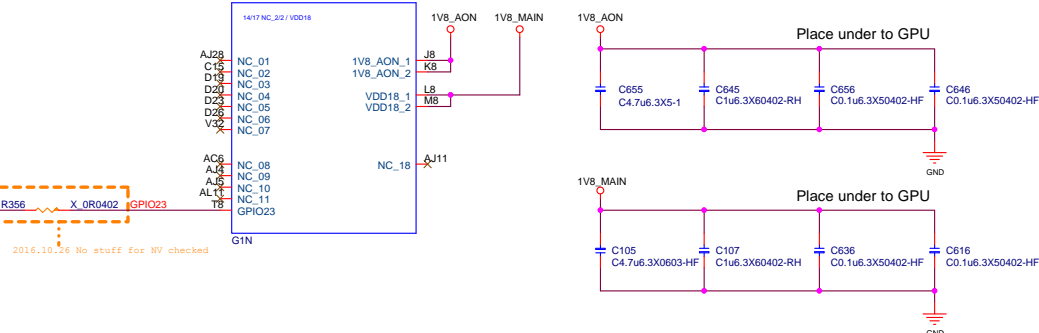
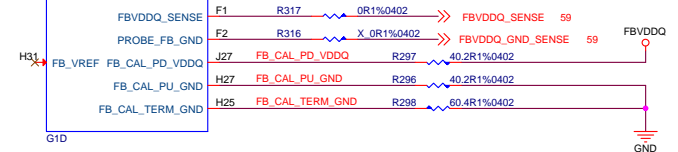
Vinafix.com



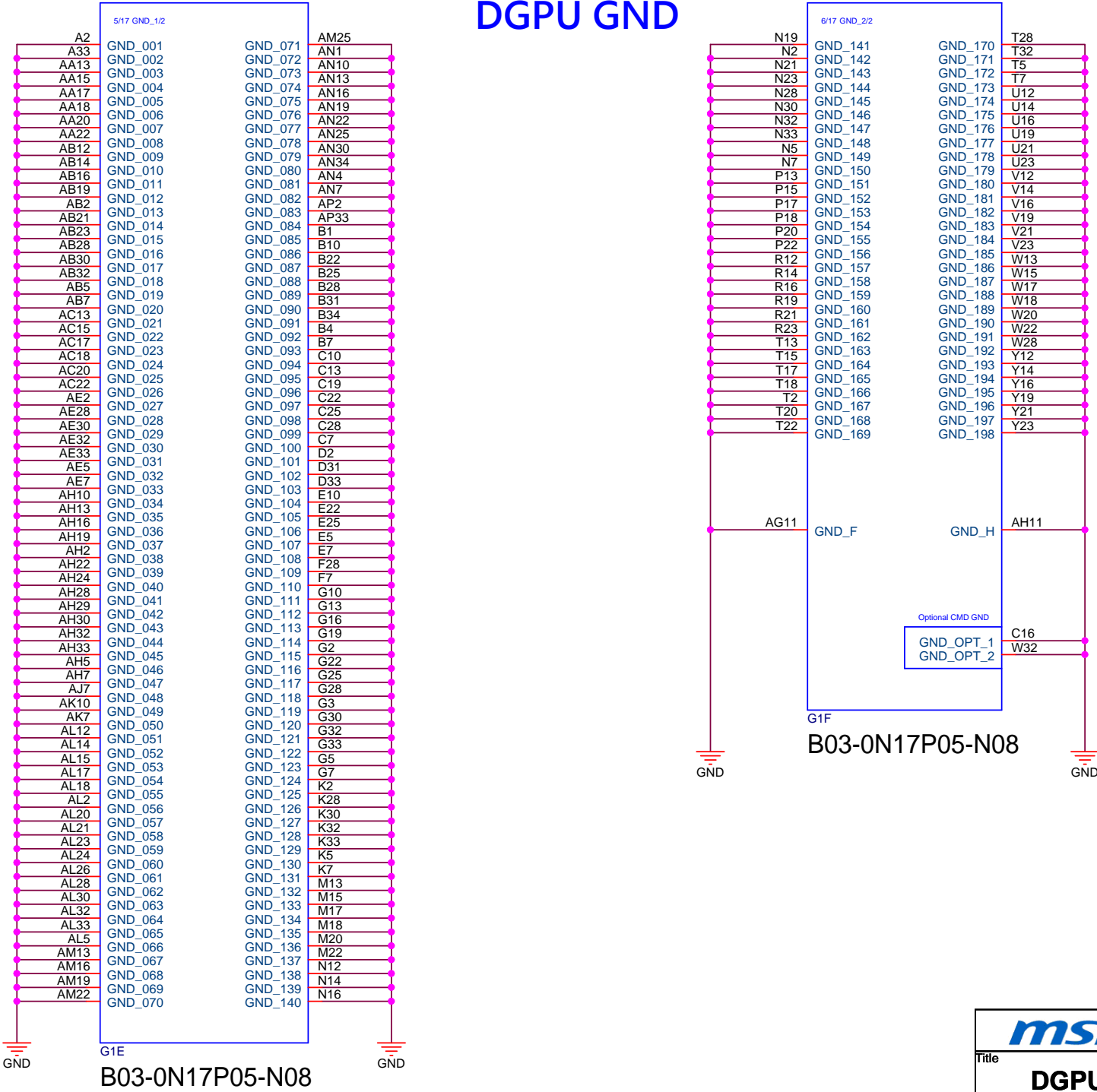
B03-0N17P05-N08



B03-0N17P05-N08

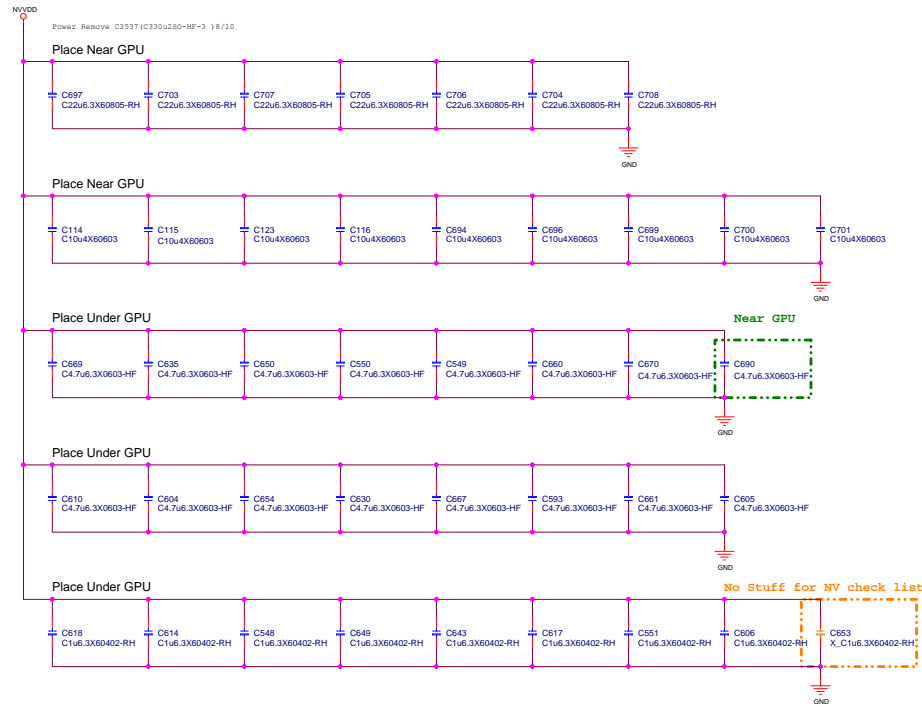


DGPU GND



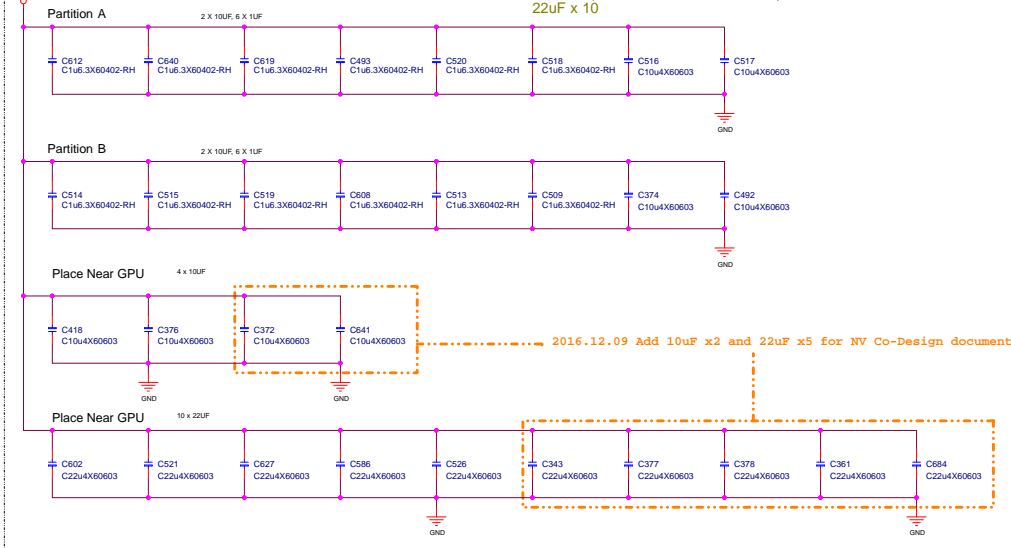
NVVD

22uF x 7
10uF x 9
4.7uF x 16 (15 Under GPU , 1 Near GPU)
1uF x 8



FBVDDQ

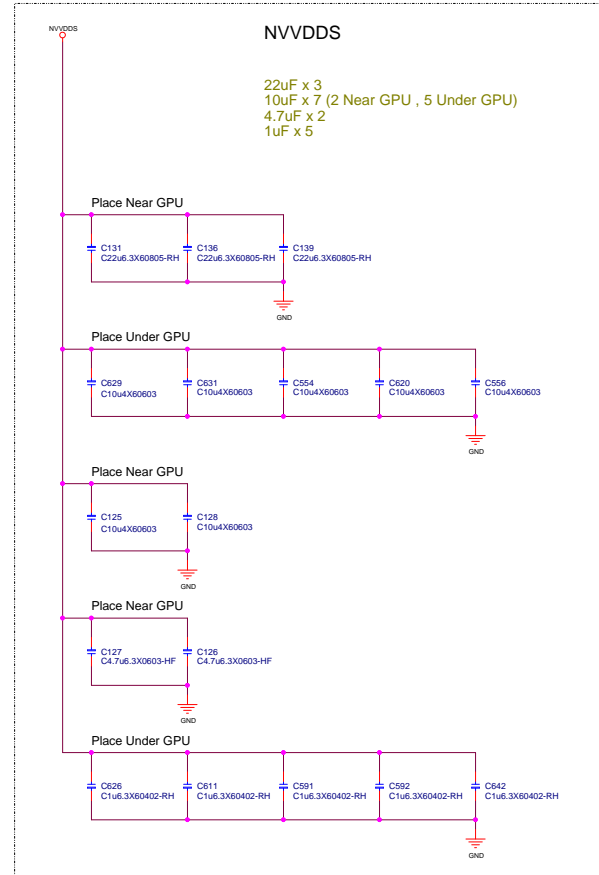
1uF x 12
10uF x 8 (4 Under GPU , 4 Near GPU)
22uF x 10



GPU DECOUPLING

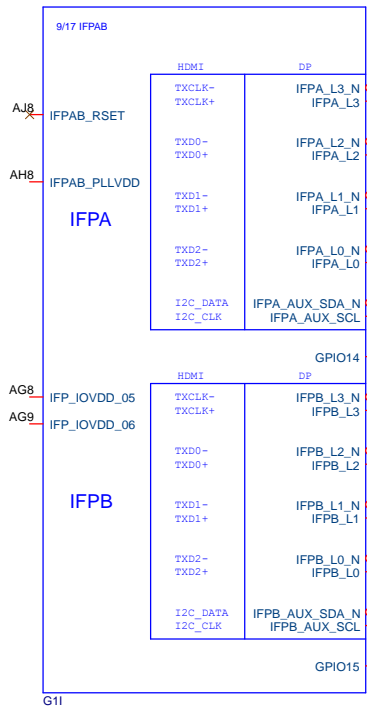
NVVD

22uF x 3
10uF x 7 (2 Near GPU , 5 Under GPU)
4.7uF x 2
1uF x 5

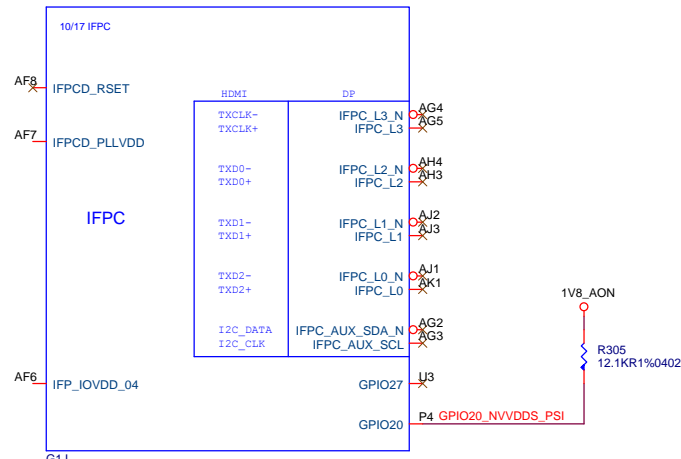


Vinafix.com

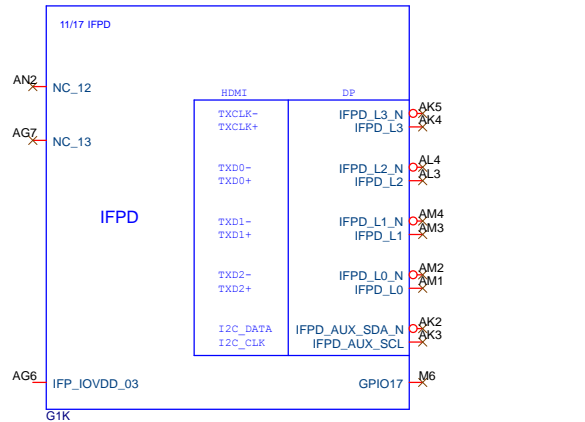
DACA,Display IF



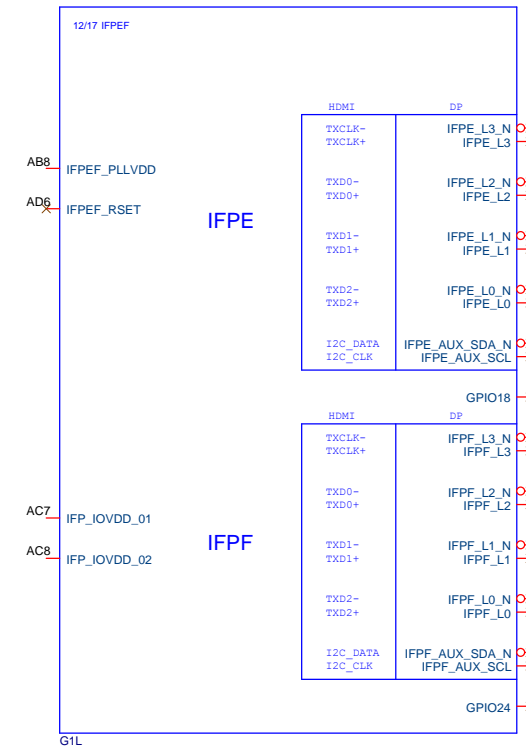
B03-0N17P05-N08



B03-0N17P05-N08



B03-0N17P05-N08

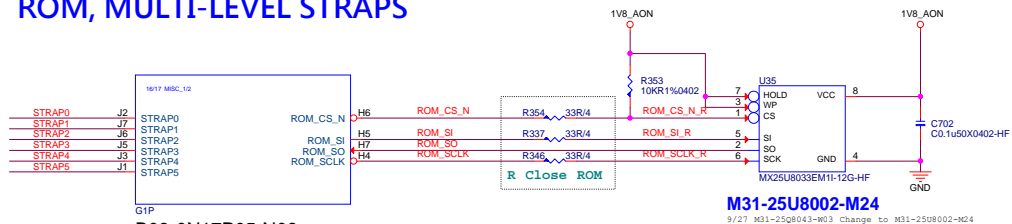


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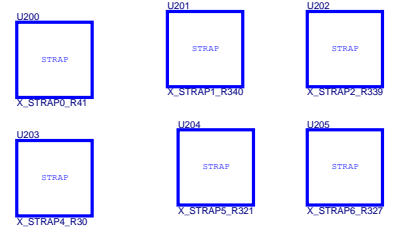
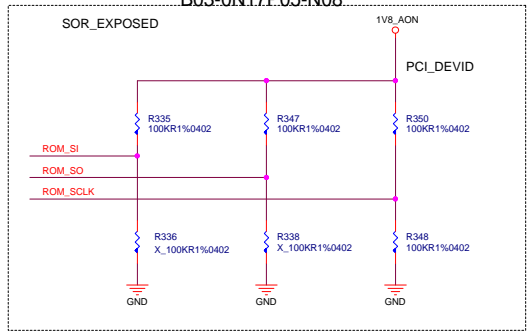


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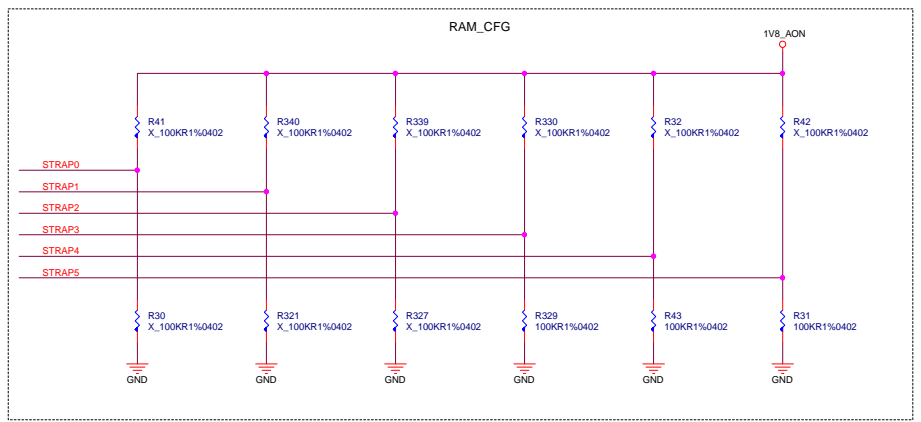
ROM, MULTI-LEVEL STRAPS



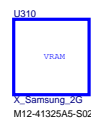
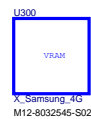
B03-0N17P05-N08



修改對應名稱 ~



STRAP0	STRAP1	STRAP2	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	R30, R321, R327
H	L	L	0x1 Micron: MT51J256M32HF-70:A	R41, R321, R327
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R30, R340, R327
H	H	L		
L	L	H		
H	L	H		
L	H	H	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R30, R340, R339
H	H	H	0x7 Samsung: M12-41325A5-S02 / K4G41325FE-HC28	R41, R340, R339
M	L	L	0x8 Micron: EDW4032BABG-70-F:A	R30, R41, R321, R327
L	M	L		



ROM_SO	ROM_SI	ROM_SCLK	SOR_EXPOSED[3:0]	1:ENABLE 0:DISABLE
L	L	L	1111 DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110	
L	H	L	1101	
L	H	H	1100	
H	L	L	1011	
H	L	H	1010	
H	H	L	1001	
H	H	H	1000	
L	L	M	0111	
L	M	L	0110	
L	M	H	0101	
L	H	M	0100	
H	L	M	0011	
H	M	L	0010	
H	M	H	0001	
H	H	M	0000	V

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

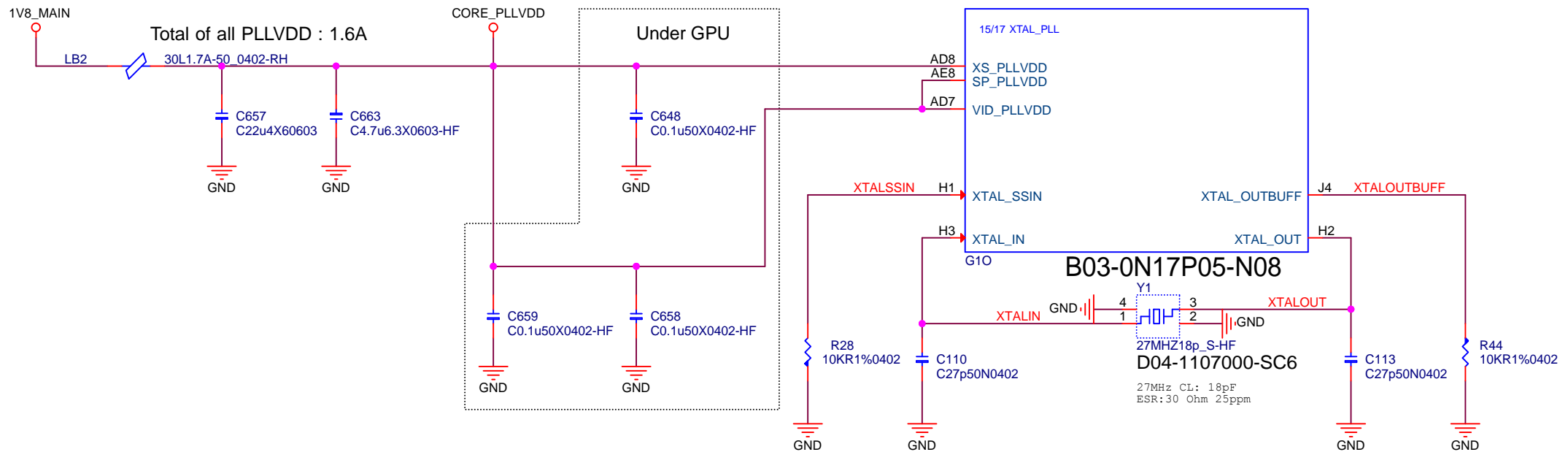
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

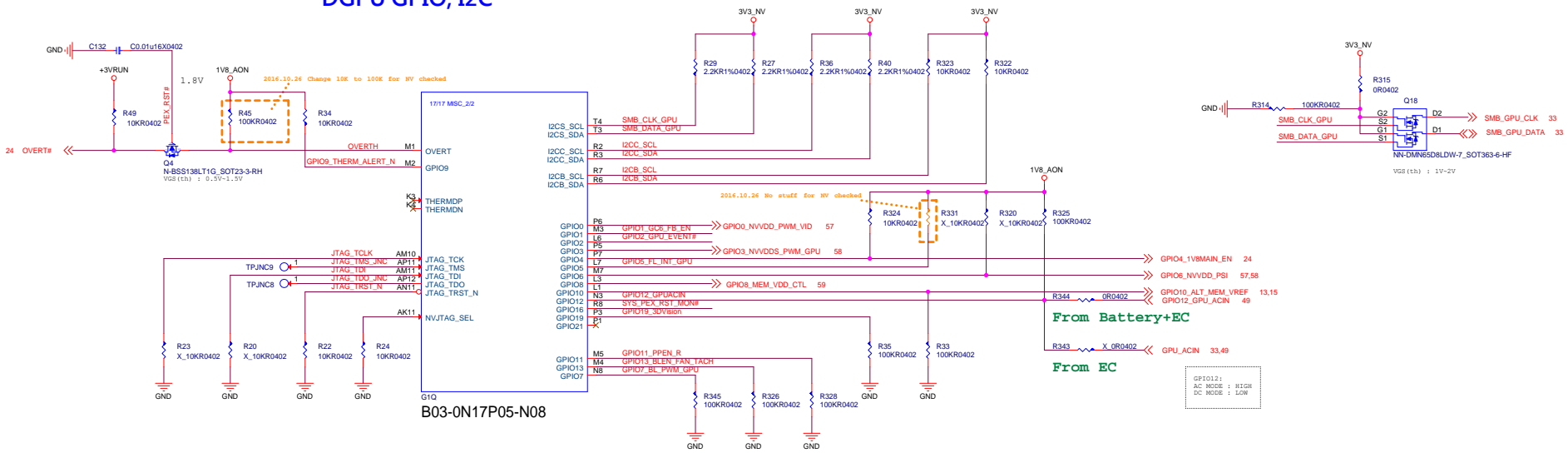
S2 G1 : U310
S2 G0 : U310 G100
S4 G1 : U300
S4 G0 : U300 G100

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

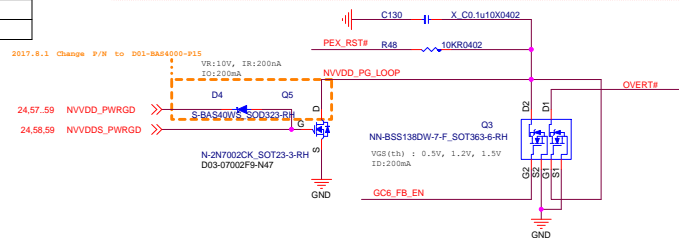
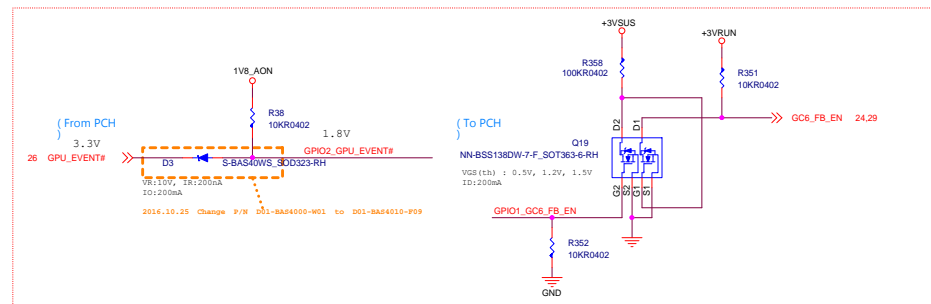
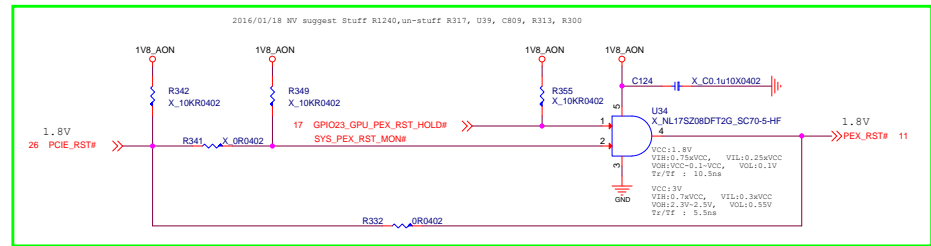
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DGPU GPIO, I2C

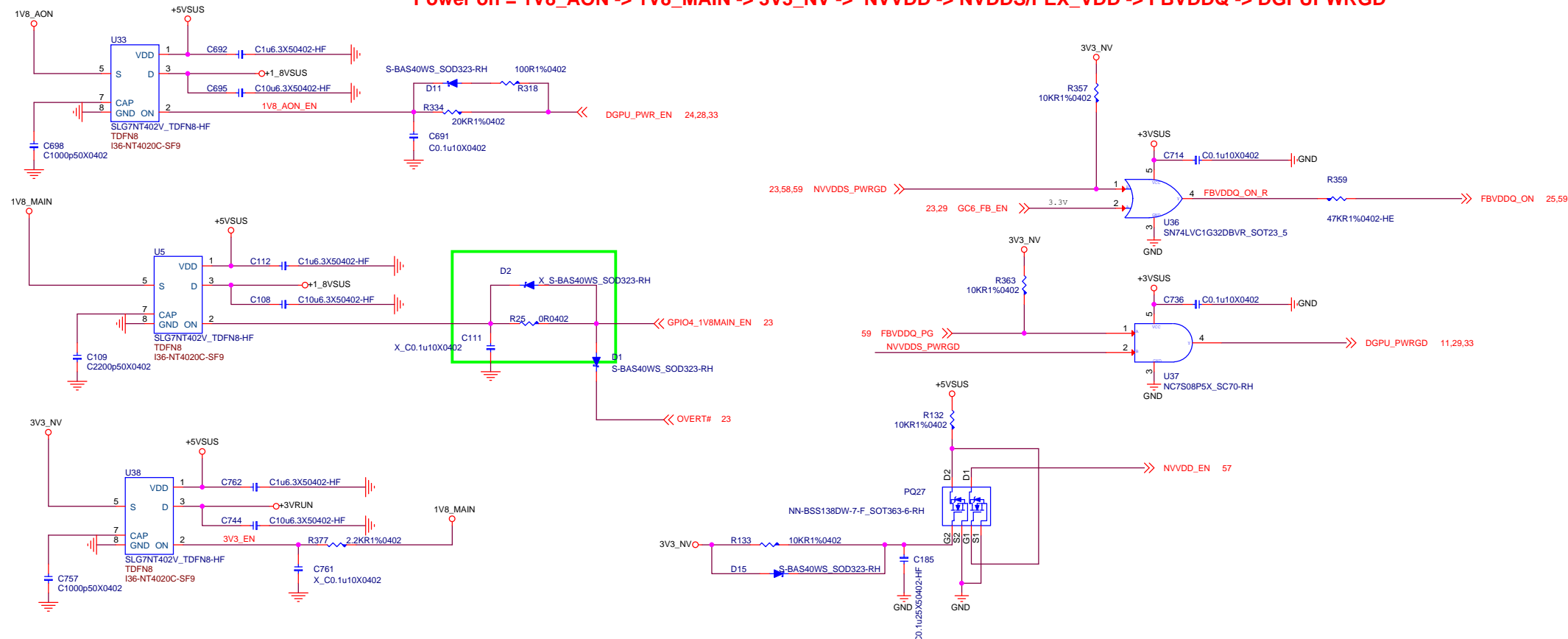


Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVDD_SRAM_FWM	O	FWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8 _AON
GPIO6	NVDD_PSI	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_FWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the 3V00/0 power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3DVision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	



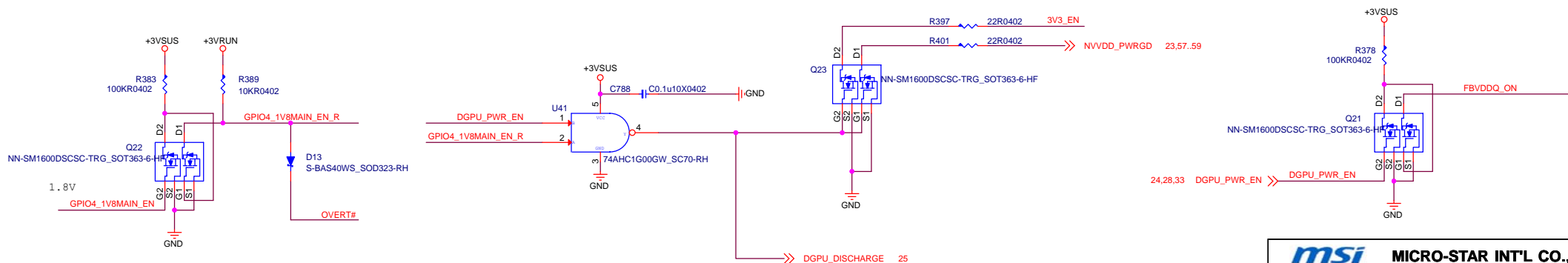
nVIDIA Power Sequence Control

Power on = 1V8_AON -> 1V8_MAIN -> 3V3_NV -> NVVDD -> NVDDS/PEX_VDD -> FBVDDQ -> DGPUPWRGD

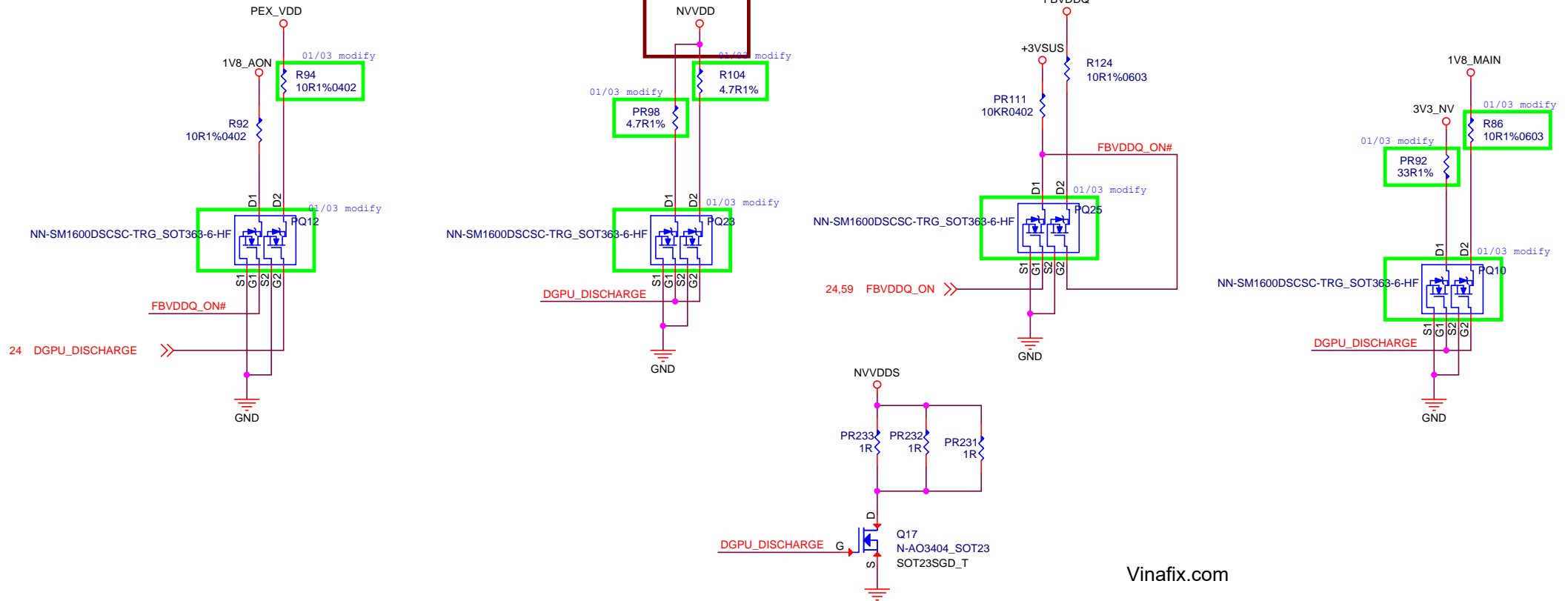


nVIDIA Power Sequence Power Down

Power down = FBVDDQ -> NVDDS/PEX_VDD -> 3V3_NV -> 1V8_AON -> 1V8_MAIN



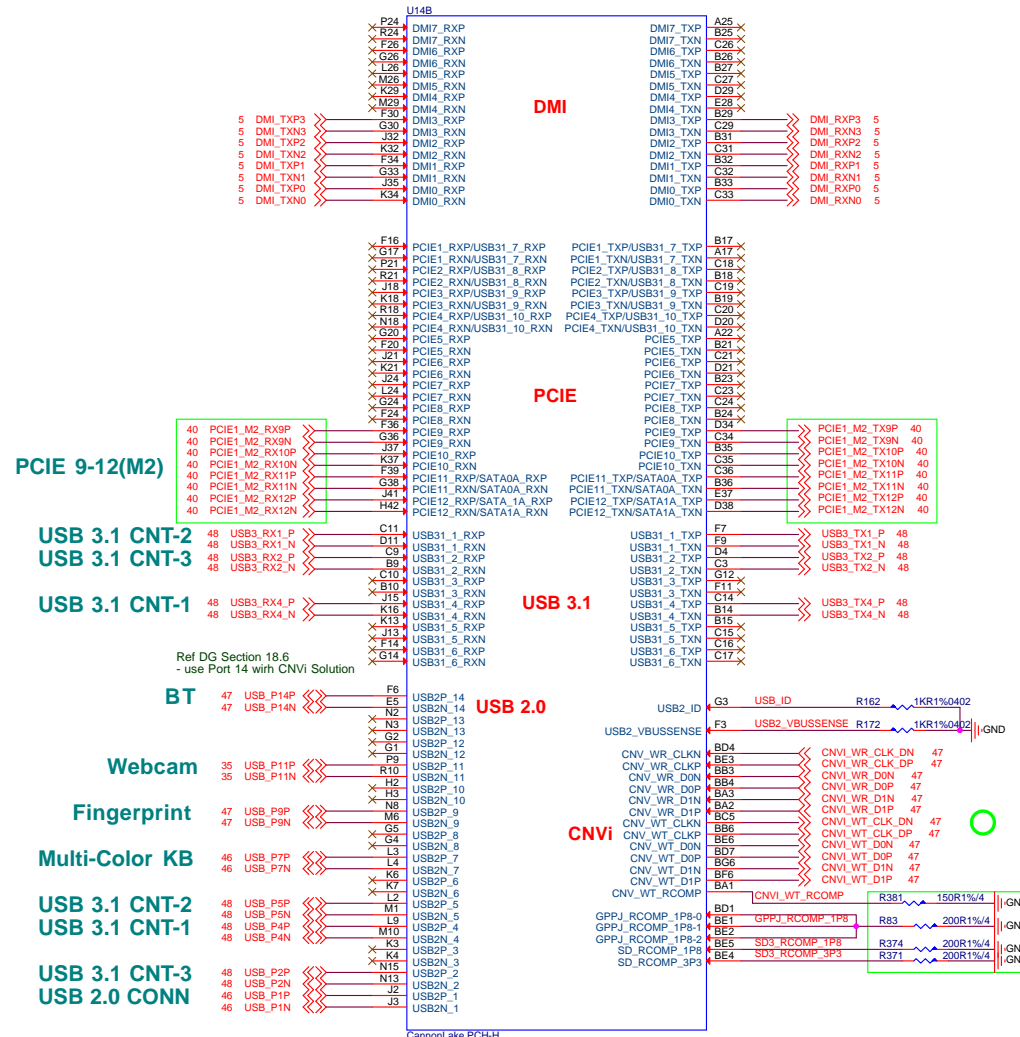
Discharge



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msi MICRO-STAR INT'L CO.,LTD.	
Title	
DGPU Power Discharge	
Size	Document Number
	MS-16K61/17B61
Date:	Wednesday, October 18, 2017
Sheet	25 of 74
Rev	0B

HM370 (DMI/PCIE/USB3.1/USB2.0/CNVi)



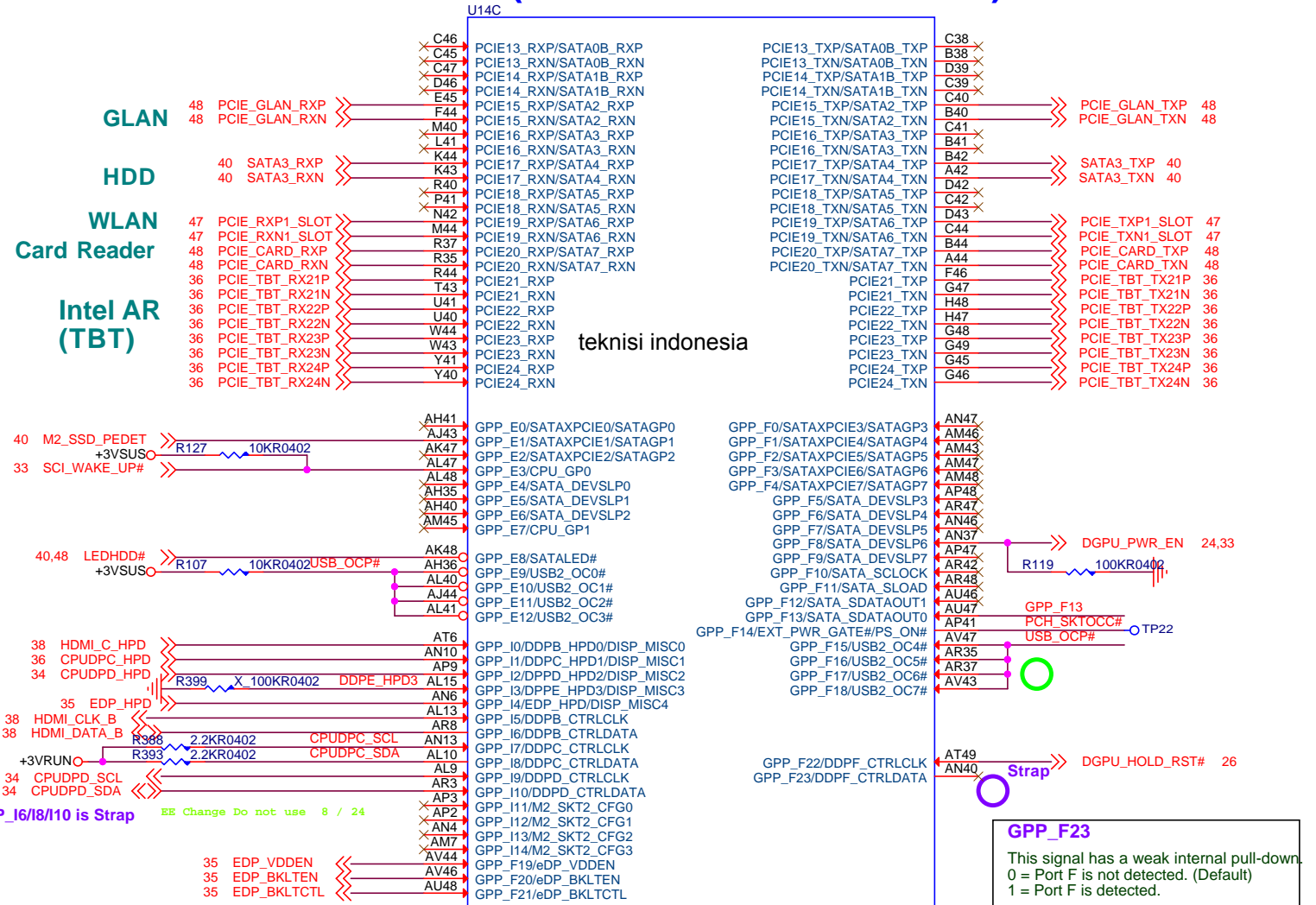
Flex I/O Lane	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
High Speed I/O (HSIO) Type and Lane	USB3.1 #1	USB3.1 #2	USB3.1 #3	USB3.1 #4	USB3.1 #5	USB3.1 #6	USB3.1 #7	USB3.1 #8	USB3.1 #9	USB3.1 #10	PCIe* #5				PCIe* #9		PCIe* #11	PCIe* #12	PCIe* #13	PCIe* #14	PCIe* #15	PCIe* #16	PCIe* #17	PCIe* #18	PCIe* #19	PCIe* #20	PCIe* #21	PCIe* #22	PCIe* #23	PCIe* #24
							PCIe* #1	PCIe* #2	PCIe* #3	PCIe* #4	GBE				GBE		SATA 0a	GBE	SATA 1a	SATA 0b	SATA 1b	SATA 2	SATA 3	SATA 4	SATA 5					
Intel® RST Support							No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	No Support	Yes			No Support	No Support	No Support	Yes				Yes			Yes	

SKU	HM370	QM370	CM370	USBS1.1 Gen1	USBS1.1 Gen2	USBS1.1 Gen3	USBS1.1 Gen4	USBS1.1 Gen5	USBS1.1 Gen6	USBS1.1 Gen7	USBS1.1 Gen8	USBS1.1 Gen9	USBS1.1 Gen10	USBS1.1 Gen11	USBS1.1 Gen12	USBS1.1 Gen13	USBS1.1 Gen14	USBS1.1 Gen15	USBS1.1 Gen16	USBS1.1 Gen17	USBS1.1 Gen18	USBS1.1 Gen19	USBS1.1 Gen20	USBS1.1 Gen21	USBS1.1 Gen22	USBS1.1 Gen23	USBS1.1 Gen24	USBS1.1 Gen25	USBS1.1 Gen26	USBS1.1 Gen27	USBS1.1 Gen28	USBS1.1 Gen29
	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN	LAN

- Added 4 new PCIe 3.0 lanes versus KBL-H platform.
- GbE LAN removed from lane 10 and SATA #0/#1 option moved from lanes 15/16 to 19/20 to better balance PHY clocking.

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HM370(SATA/PCIE/USB_OC/DDI)



HM370 (HDA/GPIO/TJAG)

Functional Strap Definitions

SMBALERT# / GPP_C2

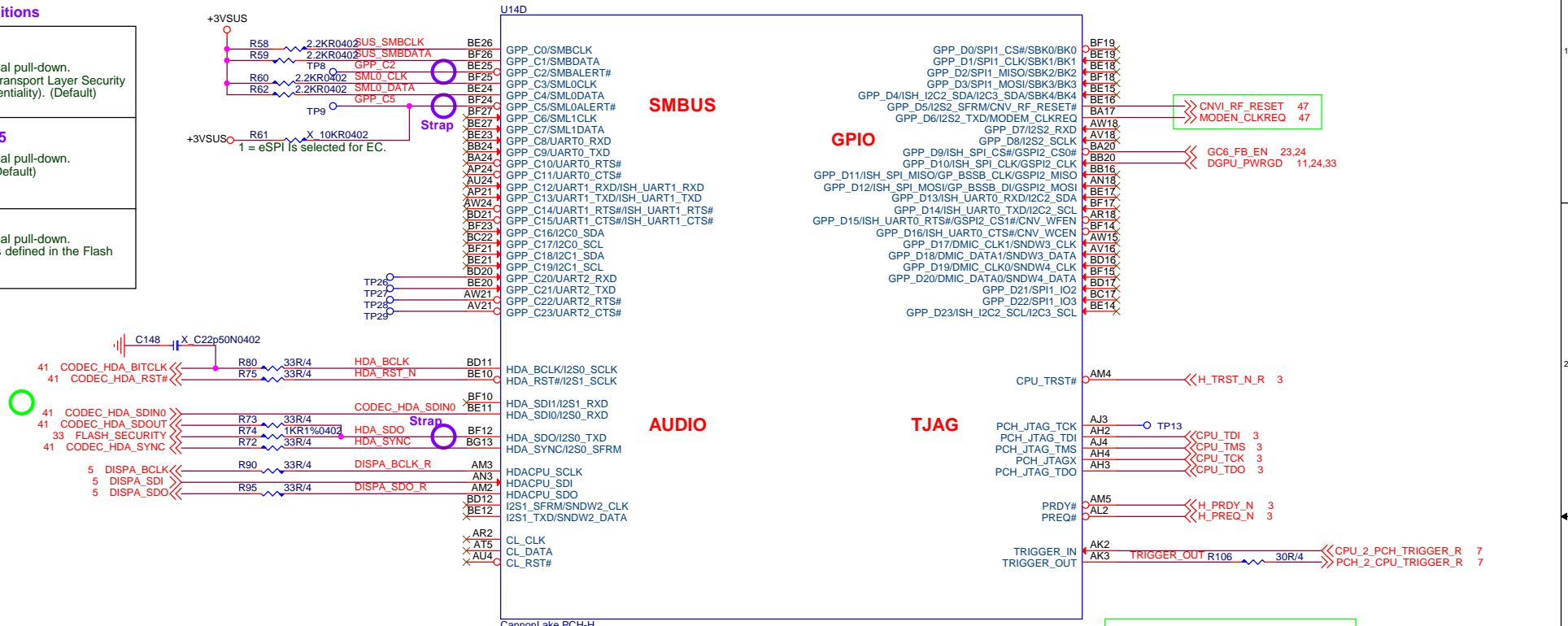
This signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)

SML0ALERT# / GPP_C5

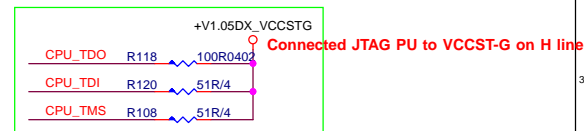
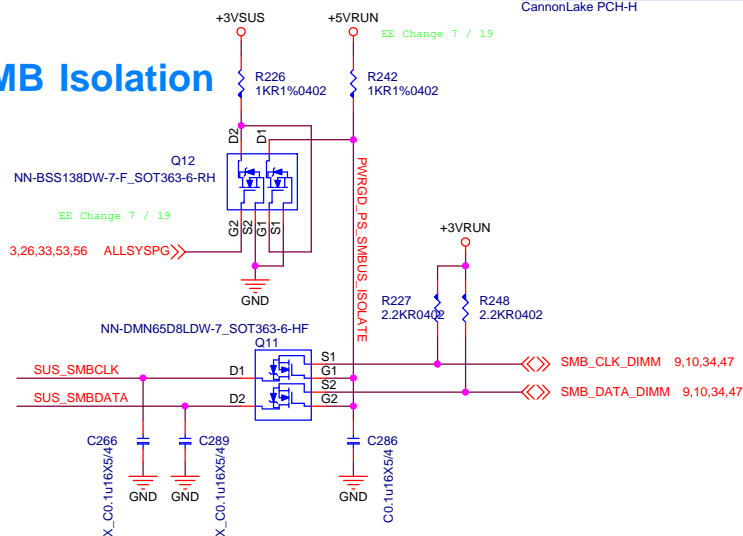
This signal has a weak internal pull-down.
0 = LPC Is selected for EC. (Default)
1 = eSPI Is selected for EC.

HDA_SDO

This signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor. (Default)

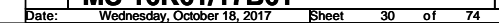


SMB Isolation



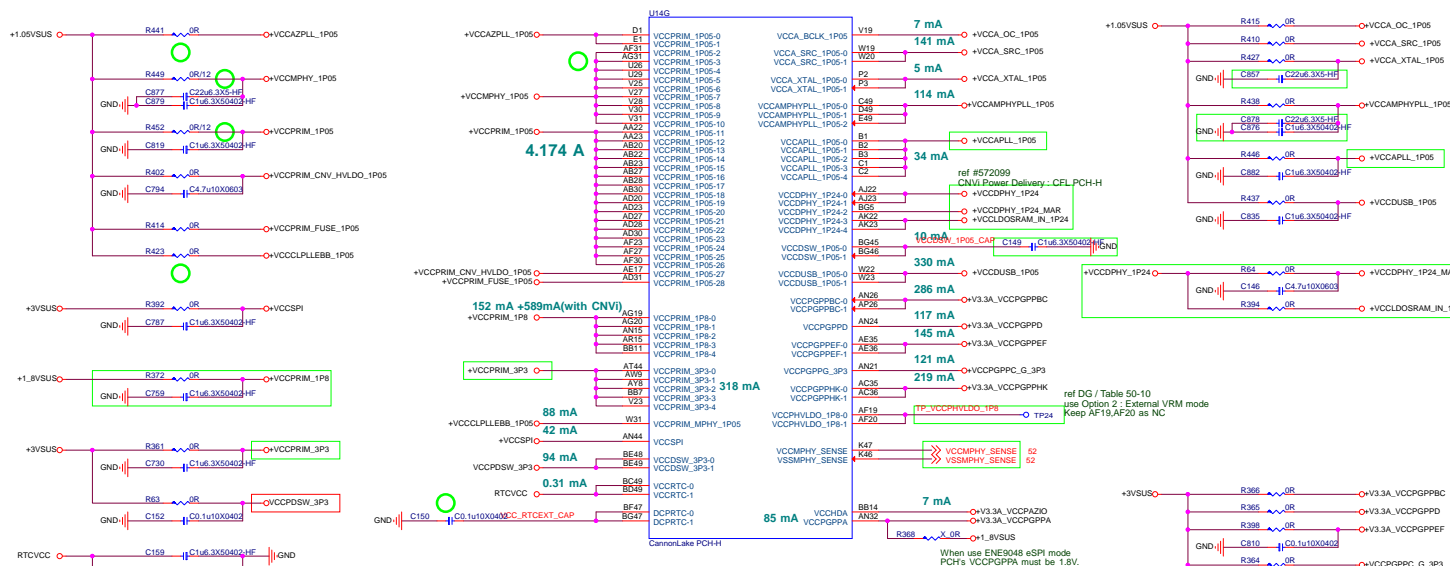
ref DG / Chapter Platform and Test Hooks
CPU_TDO : PU 100R Near CPU (DG : R1)
PU 100R Near PCH (DG : R3)
CPU_TDI : PU 51R Near PCH (DG : R4)
CPU_TMS : PU 51R Near PCH (DG : R5)
CPU_TCK : 51R to GND Near CPU (DG : R2)

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HM370 (Power)

ref DG / Table 50-6 Decoupling Requirements



GPIO Group Summary

GPIO Group	Power Pins	Voltage
Primary Well Group A (GPP_A)	VCCGPPA	1.8V or 3.3V
Primary Well Group B (GPP_B)	VCCGPPBC	1.8V or 3.3V
Primary Well Group C (GPP_C)		
Primary Well Group D (GPP_D)	VCCGPPD	1.8V or 3.3V
Primary Well Group E (GPP_E)	VCCGPPFE	1.8V or 3.3V
Primary Well Group F (GPP_F)		
Primary Well Group G (GPP_G)	VCCGPPG_3P3 or VCCPRIM_1P8	1.8V or 3.3V
Primary Well Group H (GPP_H)	VCCGPPHK	1.8V or 3.3V
Primary Well Group K (GPP_K)		
Primary Well Group I (GPP_I)	VCCPRIM_3P3	3.3V Only
Primary Well Group J (GPP_J)	VCCPRIM_1P8	1.8V Only
Deep Sleep Well Group (GPD)	VCCDSD_3P3	3.3V Only

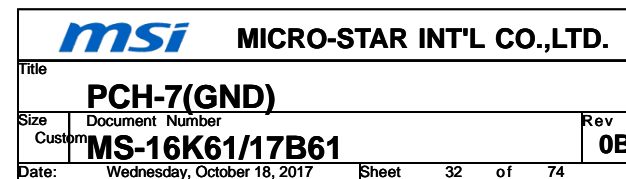
Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

Note: Except for GPP_G group, the operating voltage of a GPIO group having voltage configurability (3.3V or 1.8V) is selected by both connecting the corresponding power pin and setting the group-voltage-selection soft strap to the desired voltage. GPP_G group voltage is selected by setting the corresponding soft strap only.

Power Descriptions for PCH in CNL-H

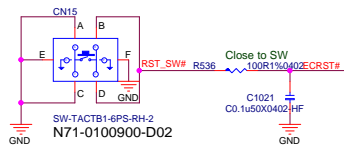
Name	Description
VCCA_BCLK_1P05	Analog supply for BCLK circuitries: 1.05V
VCCA_SRC_1P05	Analog supply for PCIe clock circuitries: 1.05V
VCCA_XTAL_1P05	Analog supply for XTAL circuitries: 1.05V
VCCDUSB_1P05	Supply for USB digital logic: 1.05V
VCCAPLL_1P05	Analog supply for BCLK/DMI/Audio PLLs: 1.05V. This rail can be derived from the VCCPRIM_1P05 rail with the proper isolation. Refer to the Platform Design Guide for implementation detail.
VCCPRIM_1P05	Primary Well: 1.05V. For PCIe/U/USB3/SATA MPHY logic, I/O blocks, SRAM, JTAG, CNVI. Deep Sx Well: 1.05V. This rail is generated by on die DSW low dropout (LDO) linear regulator to supply DSW core logic. Board needs to connect a 1uF capacitor to this rail and power should NOT be driven from the board.
VCCPRIM_MPHY_1P05	MOD PHY Primary: 1.05V. Primary supply for PCIe/USB3/SATA MPHY logic and PCIe/USB PLL dividers.
VCCAMPHYPLL_1P05	Analog supply for USB3, PCIe Gen 2/Gen 3, and SATA3 PLLs: 1.05V. Refer to the Platform Design Guide for filtering and decoupling recommendations.
VCCPRIM_1P8	1.8V Primary Well.
VCCPRIM_3P3	3.3V Primary Well.
VCCSPI	SPI Primary Well 3.3V or 1.8V, for SPI interface.
VCCHDA	HDA Audio Power 3.3V, 1.8V, or 1.5V, for Intel® High Definition Audio.
VCCDSW_3P3	3.3V Deep Sx Well.
VCCRTC	RTC Well Supply. This rail can drop to 2.0V if all other planes are off. This power is not expected to be shut off unless the RTC battery is removed or drained.
	Note: VCCRTC nominal voltage is 3.0V. This rail is intended to always come up first and always stay on. It should NOT be power cycled regularly on non-chip battery designs. Refer to the Platform Design Guide, RTC Design Guidelines chapter for latest design recommendations.
	Note: Implementation should not attempt to clear CMOS by using a jumper to pull VCCRTC low. Clearing CMOS can be done by using a jumper on RTRCST# or GPI.
DCPRTC	RTC decoupling capacitor only. This rail should NOT be driven.
VCCDPHY_1P24	1.24V for CNVI logic. This rail is generated internally with a LDO and needs to be routed to the motherboard so that the rail can be supplied back to the SoC. Refer to the Platform Design Guide for implementation details.
VCCDPHY_EC_1P24	For decoupling capacitor only. This rail should NOT be driven from the motherboard. This rail can optionally be connected to VCCDPHY_1P24 on the motherboard.
VCCPHVLD0_1P8	1.8V Primary Well. On the motherboard, this power pin must be connected to VCCPRIM_1P8 rail in Internal 1.8 V VRM Mode and left as no-connect in External 1.8V VRM Mode.
VCCGPPA	1.8V or 3.3V for GPP_A group.
VCCGPPBC	1.8V or 3.3V for GPP_B and GPP_C groups.
VCCGPPD	1.8V or 3.3V for GPP_D group.
VCCGPPPEF	1.8V or 3.3V for GPP_E and GPP_F groups.
VCCGPPG_3P3	3.3V for GPP_G group.
VCCGPPHK	1.8V or 3.3V for GPP_H and GPP_K groups.
VCCMPHY_SENSE	1.05V Sense Line.
VSSMPHY_SENSE	0V (Ground) Sense Line.
VSS	Ground.

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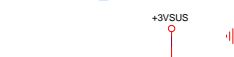
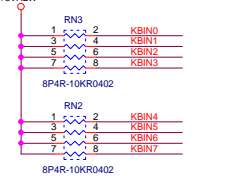
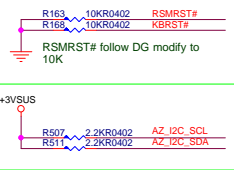


KBC/EC/uP (ENE9028)

Hardware Reset

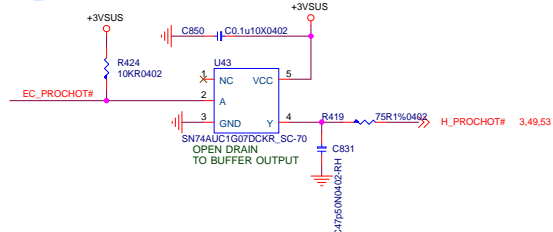


PU/PD

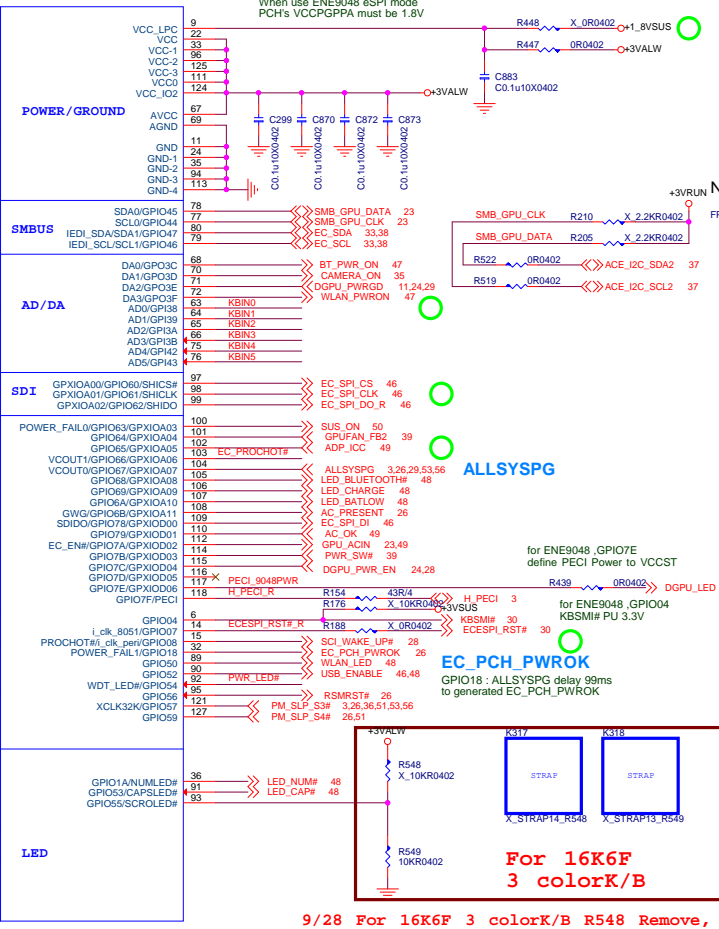
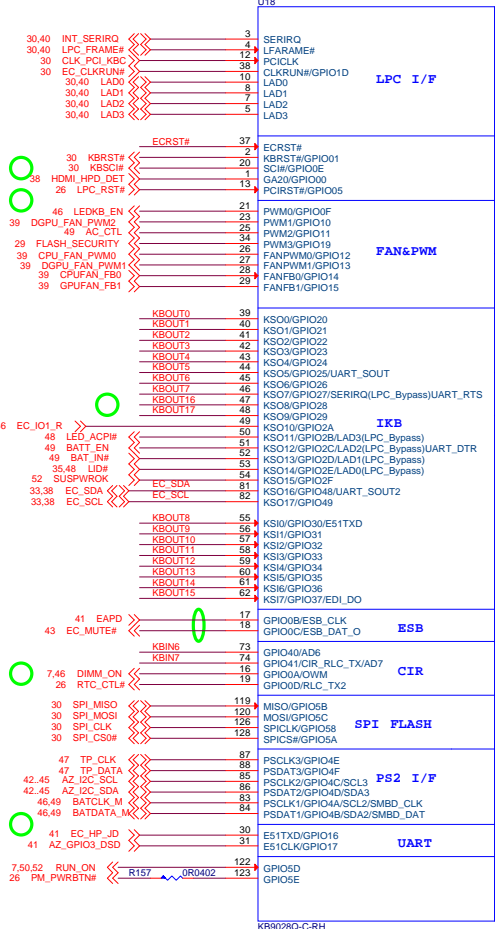
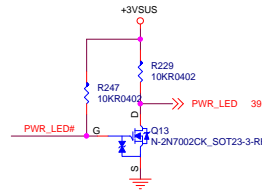


remove OVERT# (Active Low)

EC_PROCHOT#



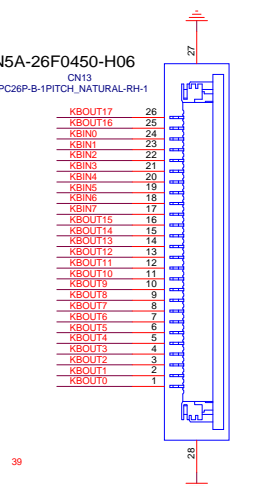
Remove MB_ID



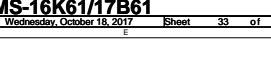
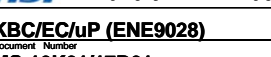
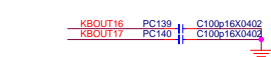
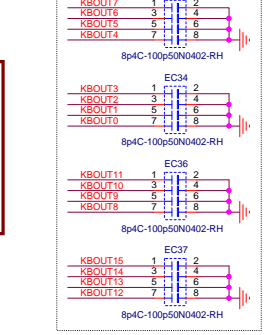
ENE9028 & 9048 Power Notes :

pin9 VCC_LPC :
3.3V for ENE9028's LPC mode.
1.8V for ENE9048's eSPI mode.

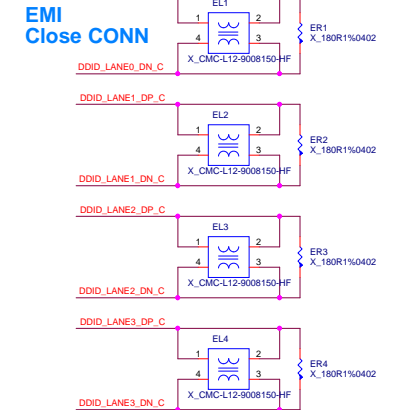
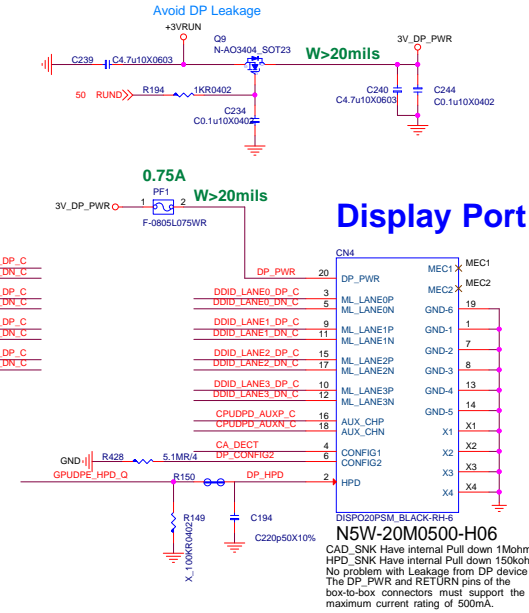
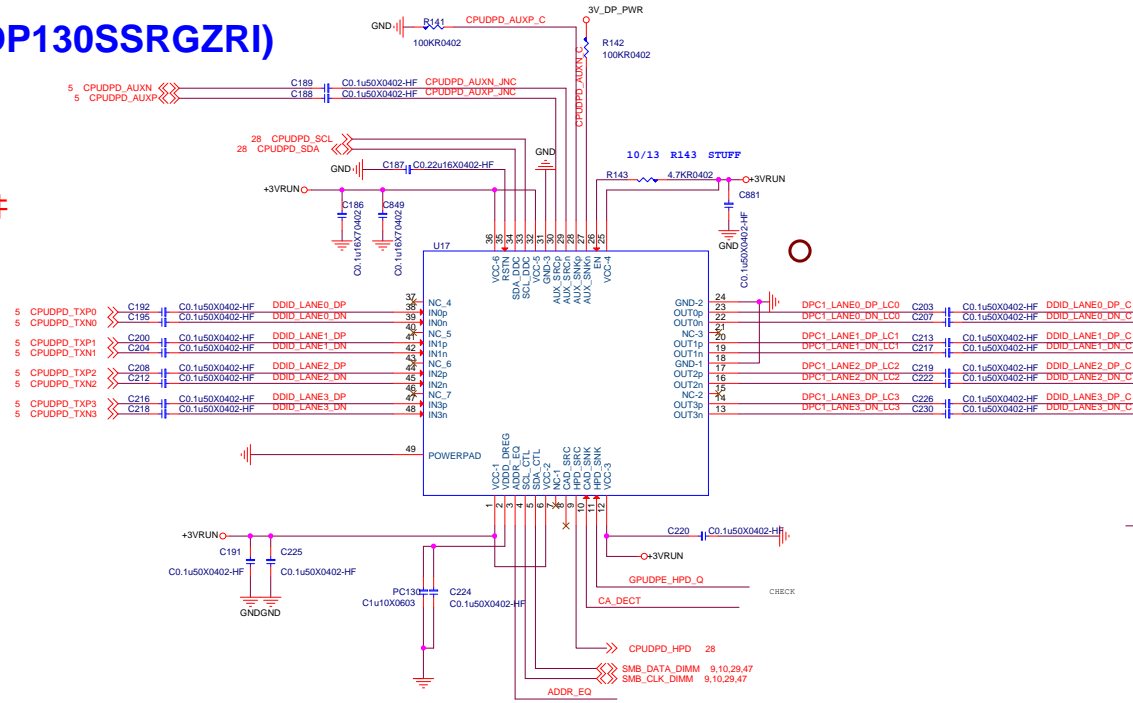
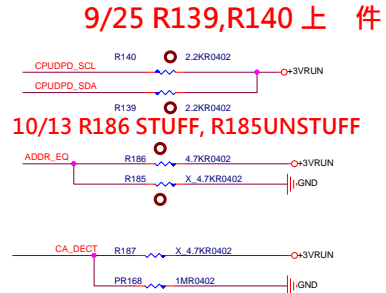
pin111 VCC0 :
3.3V for ENE9028's PLC function
3.3V for ENE9048's eSPI operation with Pre-Driver.



For EMI

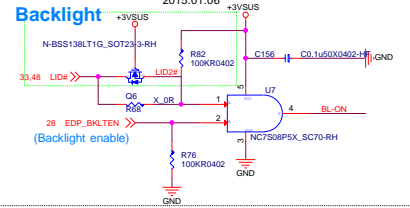
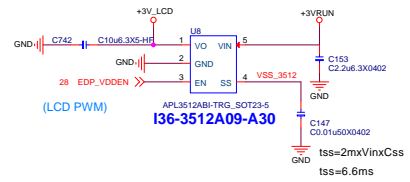


DP 1.2 Redriver (SN75DP130SSRGZRI)

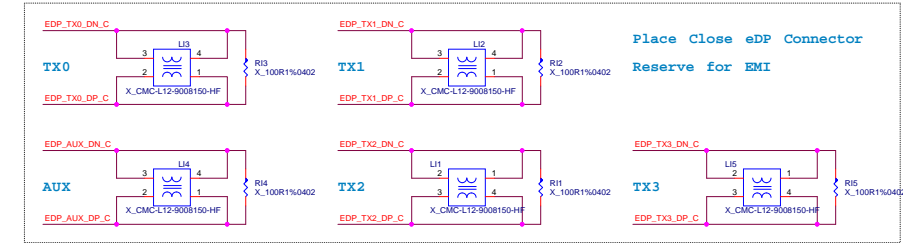
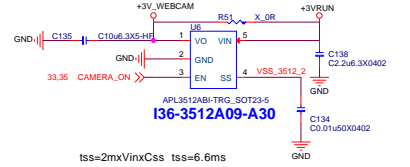


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Pannel Device Logic Power

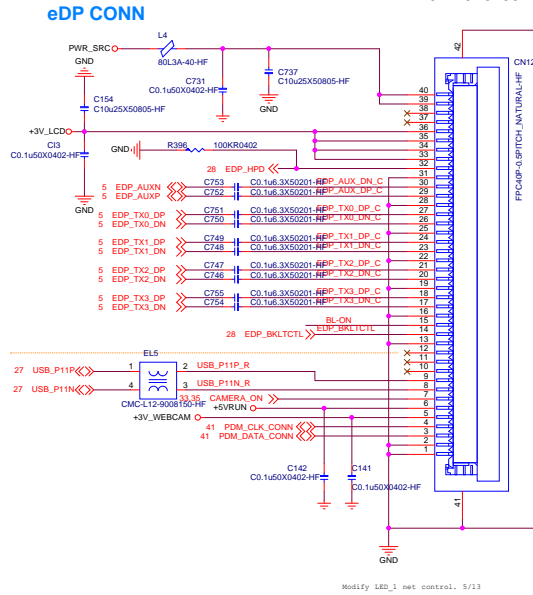


CAMERA Power



eDP Connector

N5A-40F0180-A81



LCD Module Pin Define FOR FULL HD PANEL

Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	NC	No Connection (Reserved)

LCD Module Pin Define FOR WQHD PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	NC	No Connection (Reserved)

LCD Module Pin Define FOR QHD+ PANEL

Pin No	Symbol	Description
1	NC	Reserved for LCD manufacturer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	NC	Reserved for LCD manufacturer's use
19	NC	Reserved for LCD manufacturer's use
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	VDD	LCD logic and driver power(3.3V)
23	VDD	LCD logic and driver power(3.3V)
24	VDD	LCD logic and driver power(3.3V)
25	NC	Reserved for LCD manufacturer's use
26	LCD_GND	LCD logic and driver ground
27	LCD_GND	LCD logic and driver ground
28	LCD_GND	LCD logic and driver ground
29	LCD_GND	LCD logic and driver ground
30	LCD_GND	LCD logic and driver ground
31	HPD	HPD signal pin
32	NC	Reserved for LCD manufacturer's use
33	PWM_OUT	PWM_OUT
34	PWM_IN	PWM_IN
35	NC	Reserved for LCD manufacturer's use
36	NC	Reserved for LCD manufacturer's use
37	NC	Reserved for LCD manufacturer's use
38	VBL	LED Anode
39	VBL	LED Anode
40	NC	Reserved for LCD manufacturer's use
41	LED_C1	LED Cathode 1
42	LED_C2	LED Cathode 2
43	LED_C3	LED Cathode 3
44	LED_C4	LED Cathode 4
45	LED_C5	LED Cathode 5
46	LED_C6	LED Cathode 6
47	LED_C7	LED Cathode 7
48	LED_C8	LED Cathode 8
49	NC	Reserved for LCD manufacturer's use
50	NC	Reserved for LCD manufacturer's use



Thunderbolt

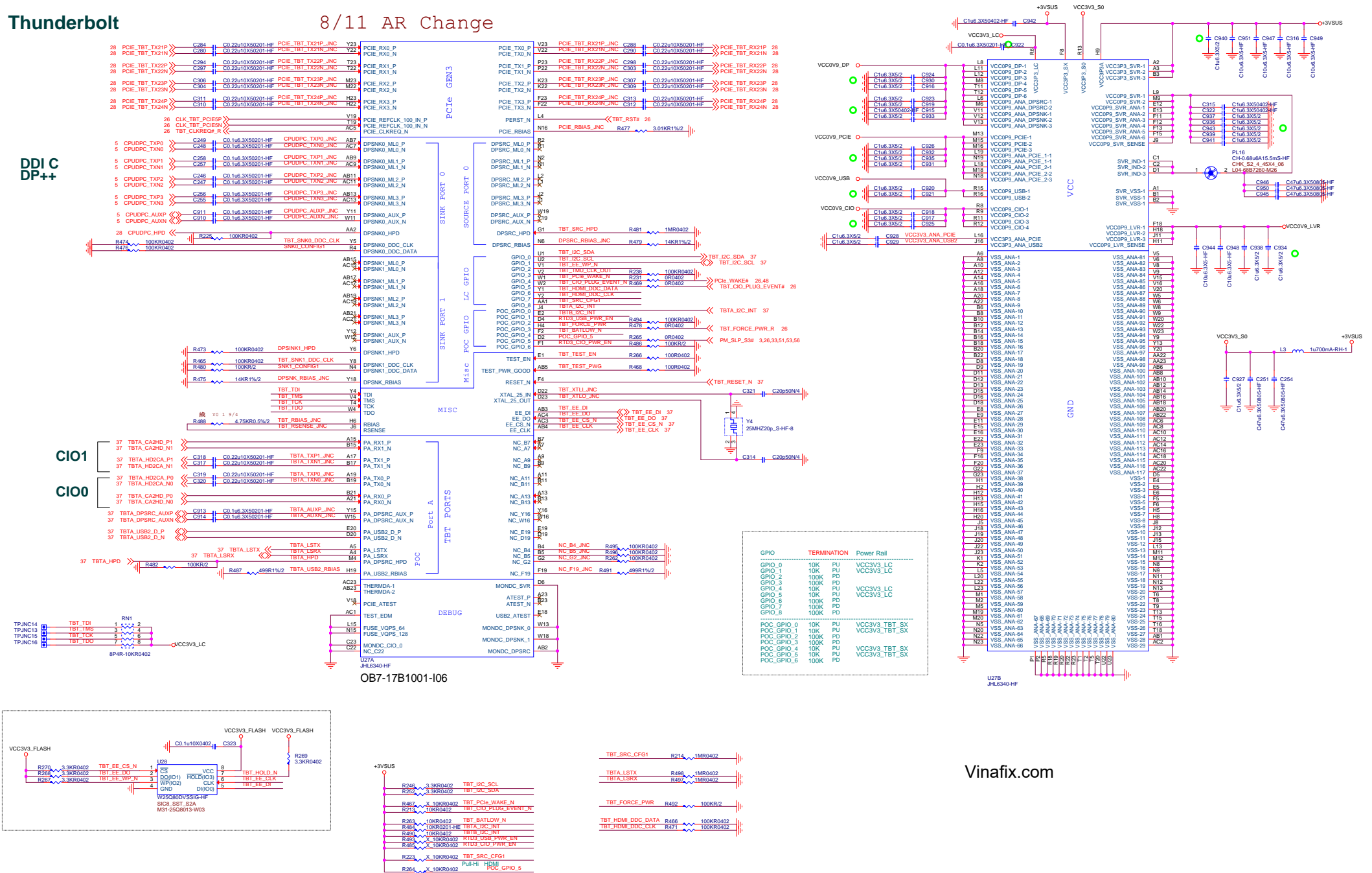
8/11 AR Change

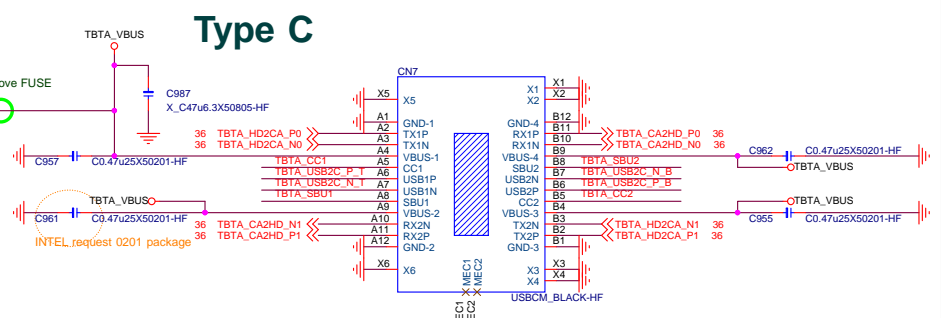
DDI C
DP++

CIO1
CIO0

OB7-17B1001-I06

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N53-24M0060-J06

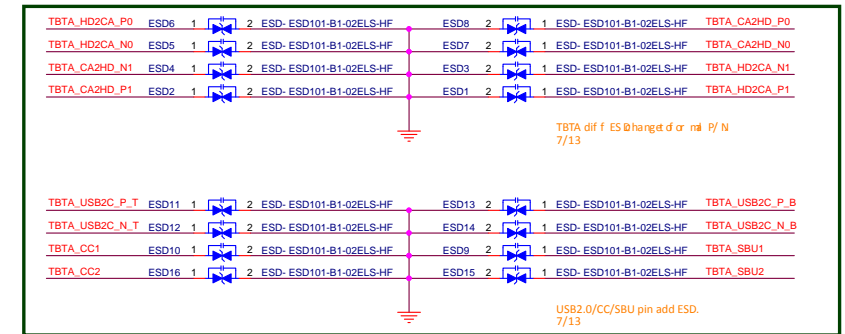
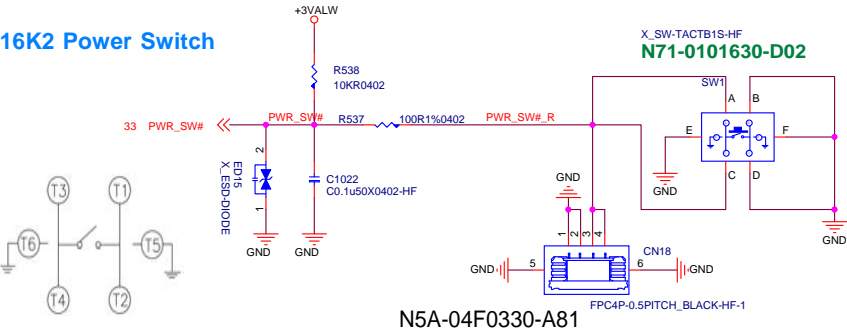


Diagram of CMC-L12-9008150-HF connector showing TBTA_USB2_N_T, TBTA_USB2_P_T, TBTA_USB2_P_B, and TBTA_USB2_N_B pins connected to a USB2.0 symbol.

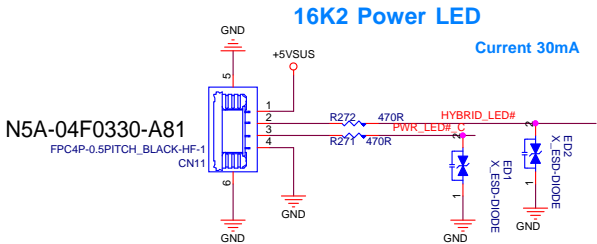
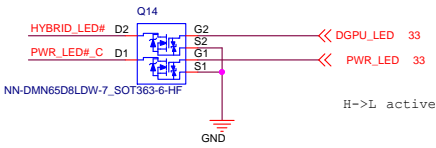
PWR SW/CPU FAN/BTB CONN/ LED CONN

16K2 Power Switch

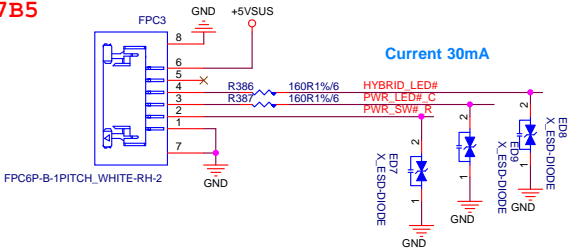


DGPU_LED	PWR_LED	LED COLOR
L	H	RED
H	H	ORANGE
H	L	GREEN
L	L	X

Control PWR LED

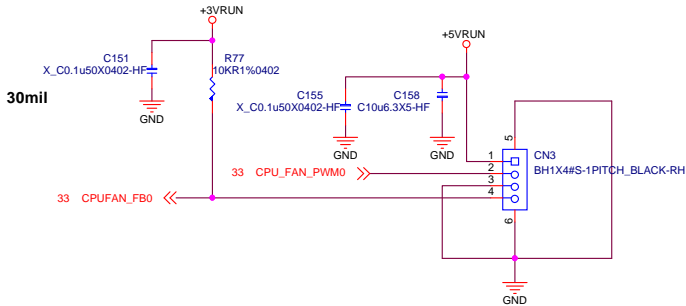


Power LED+SW For 17B5

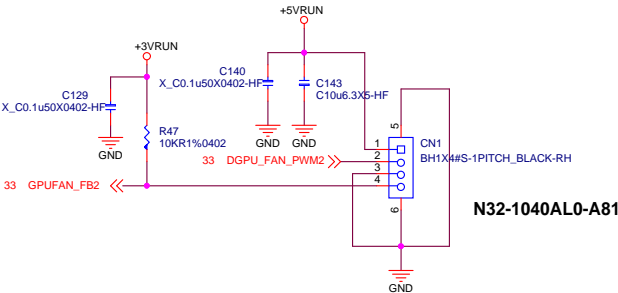
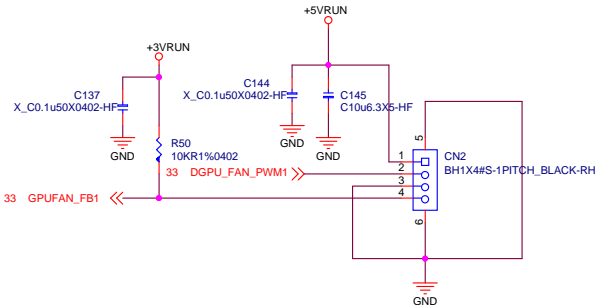


remove 16K2's LED ACPI#_BR and ACPI_BR Circuit

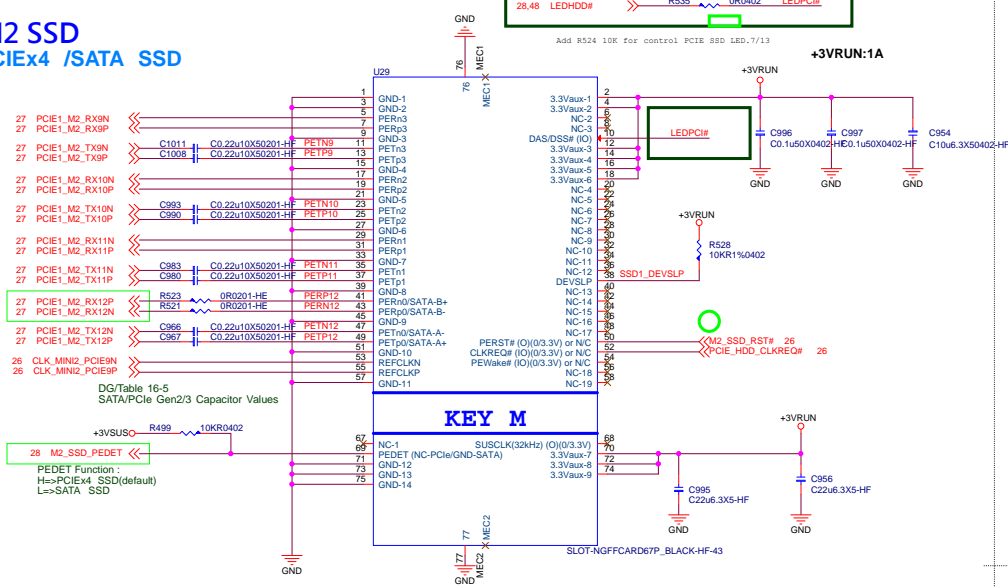
CPU FAN



DGPU FAN



M2 SSD PCIe4x4 /SATA SSD



AUDIO(ALC1220)

ALC1220	AZ_GPIO3_DSD
PCM	H
Native DSD	L
DOP DSD	L

To EC
To EC

To EC
Internal Mic

For 17B6

For 16K6F 3 colorK/B

9/27 R160,R161 Change 75 Ohm-->1K

Impedance DECT
Woffe FOR 17B6

MIC In

EMI
Close Codec


To Mux

9/29 PM Jerry 要求更新料號

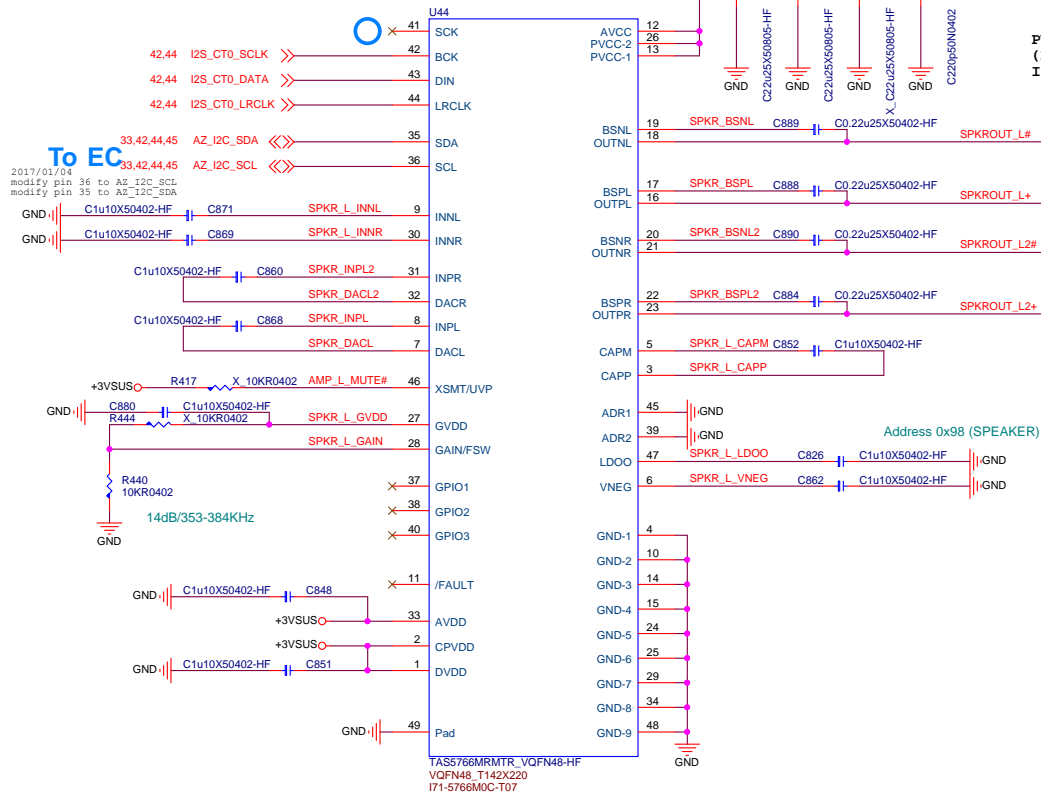


12mA

Speaker/ TI MART AMP

 MICRO-STAR INT'L CO.,LTD.	
Title	
CT5302	
Size	Document Number
Custom	MS-16K61/17B61
Date:	Wednesday, October 18, 2017
Sheet	42 of 74
Rev	0B

SMART AMP LEFT



PVCC=5V Vpp=5*2=10. Vrms=10/2.828=3.53
(RL=4 ohm) Po max =(Vrms) ^2/RL=(3.53)^2/4= 3.1W
I max=0.62 A

PVCC=19V Vpp=19*2=38. Vrms=38/2.828=13.43
(RL=4 ohm) Po max =(Vrms) ^2/RL=(13.43)^2/4= 45W
I max=2.3 A

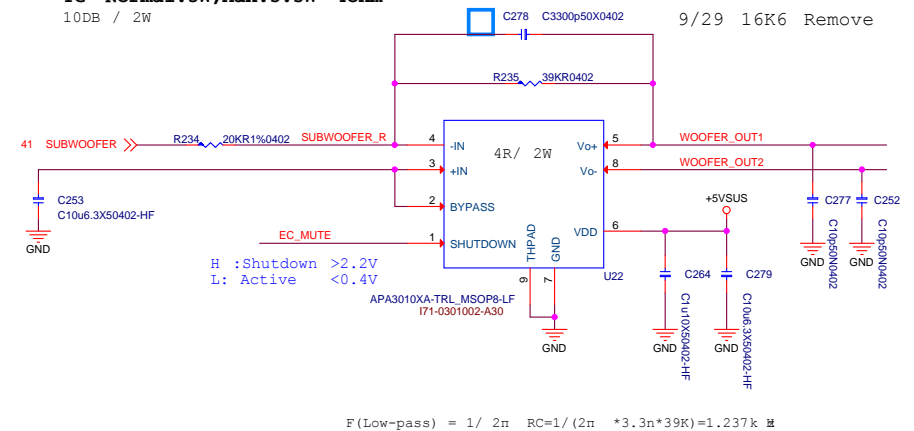
FOR 16K61

R-
R+
L-
L+

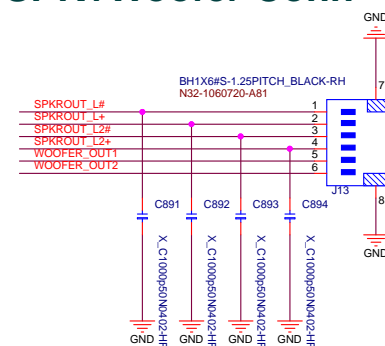
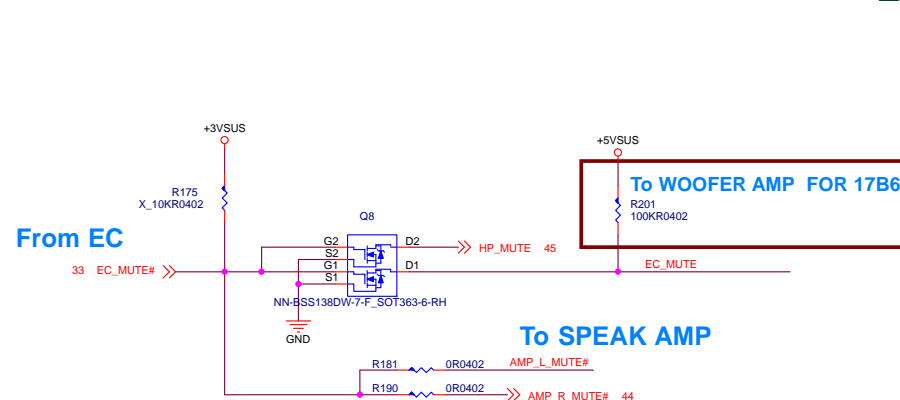
AMP WOOFER

SPK L2 / Woffer FOR 17B6

YG Normal: 3W, Max: 3.5W 4ohm
10DB / 2W



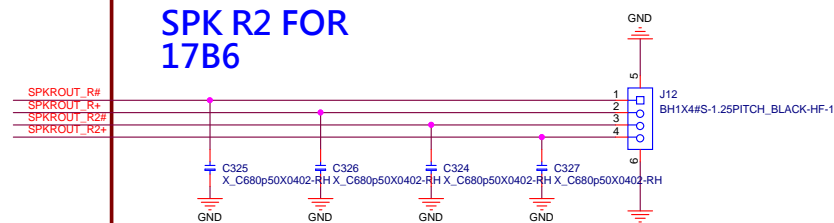
Left SPK+Woofer Conn



PCB layout for the TASS766MRMTR VQFN48-HF package, showing connections to a microcontroller (U49) and various peripheral components. The layout includes a 14dB/353-384KHz filter, a 10KR0402 resistor, and a 10KR0402 capacitor. The package is connected to a microcontroller (U49) via a 10KR0402 resistor and a 10KR0402 capacitor. The layout also shows connections to a 3VSUS supply, a 10KR0402 resistor, and a 10KR0402 capacitor. The package is connected to a microcontroller (U49) via a 10KR0402 resistor and a 10KR0402 capacitor. The layout also shows connections to a 3VSUS supply, a 10KR0402 resistor, and a 10KR0402 capacitor.

PVCC=19V Vpp=19*2=38. Vrms=38/2.828=13.43
(RL=4 ohm) Po max =(Vrms) ^2/RL=(13.43)^2/4= 45W
I max=2.3 A

Right SPK Conn
SPK R2 FOR
17B6



ESS9118

tekniisi indonesia

ES9118EQ

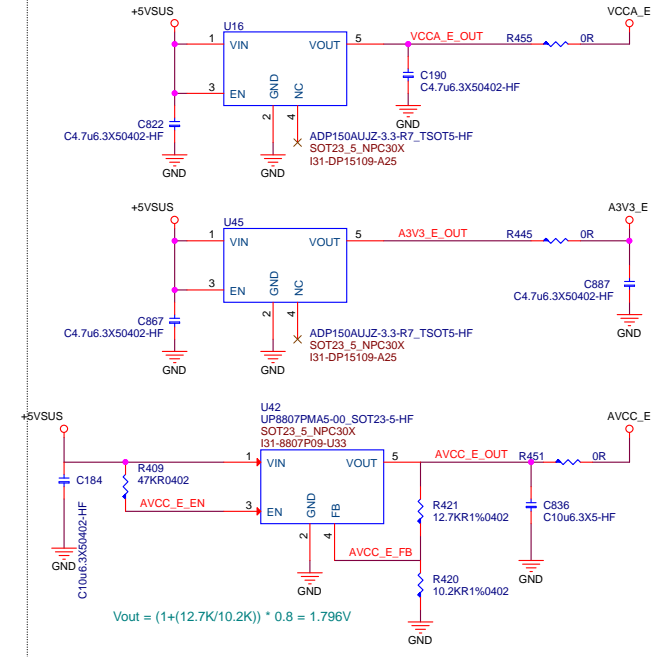
To EC

2017/01/04
modify pin 38 to A2_I2C_SCL
modify pin 39 to A2_I2C_SDA

0 = 0x90 / 1 = 0x92

Address 0x90 (ESS9118)

Power



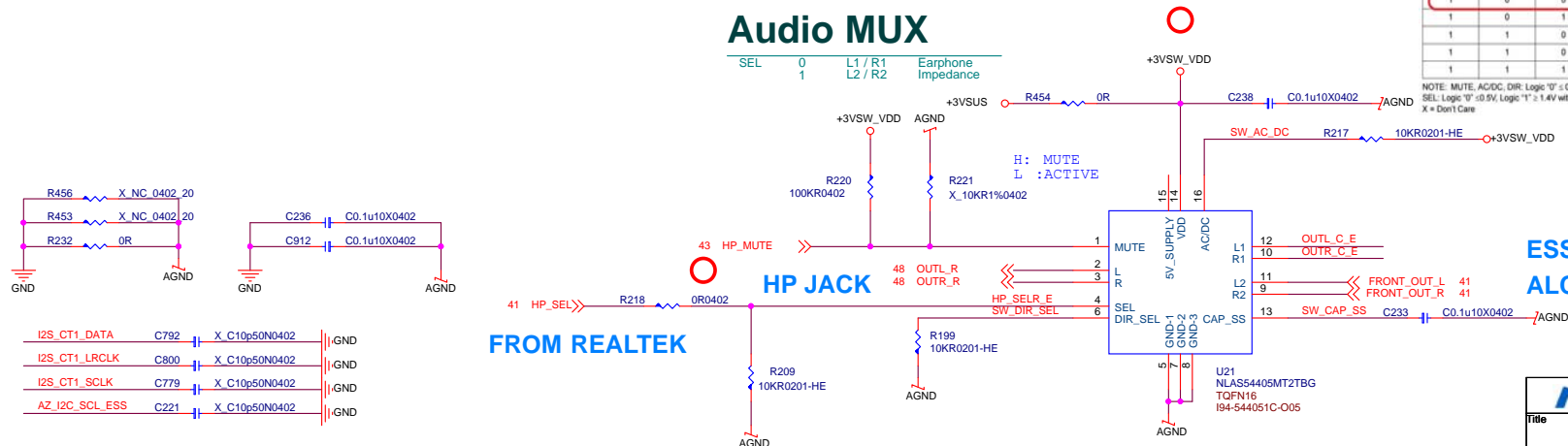
Truth Table

INPUTS				OUTPUTS					
ACDC	DIR	MUTE	SEL	L1, R1	L2, R2	COM (L,R) CIP Shunts	L1, R1 CIP Shunts	L2, R2 CIP Shunts	
0	X	0	0	ON	OFF	OFF	OFF	OFF	OFF
0	X	0	1	OFF	ON	OFF	OFF	OFF	OFF
0	X	1	X	OFF	OFF	OFF	OFF	OFF	OFF
1	0	0	0	ON	OFF	OFF	OFF	ON	ON
1	0	0	1	OFF	ON	OFF	OFF	ON	OFF
1	0	1	X	OFF	OFF	OFF	OFF	ON	ON
1	1	0	0	ON	OFF	OFF	OFF	OFF	OFF
1	1	0	1	OFF	ON	OFF	OFF	OFF	OFF
1	1	1	X	OFF	OFF	OFF	OFF	OFF	OFF

NOTE: MUTE, ACDC, DIR: Logic "0" = 0.5V, Logic "1" = 1.4V or Float with a 3.3V Supply or 5V supply.
SEL: Logic "0" = 0.5V, Logic "1" = 1.4V with a 3.3V Supply or 5V supply.
X = Don't Care

Audio MUX

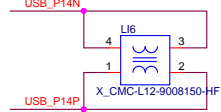
SEL 0 1 L1 / R1 L2 / R2 Earphone Impedance



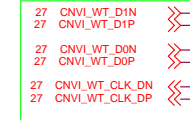
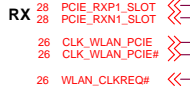
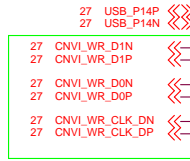
ESS9118EQ
ALC1220 IN

WLAN /ClickPad/FP

EMI

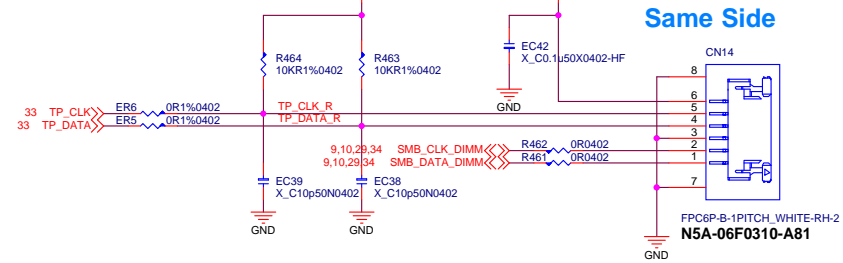


Ref DG Section 18.6
- use USB 2.0 Port 14 with CNVi Solution

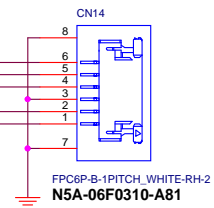


N15-0670520-L41
SLOT_NGFFCARD67P_BLACK-HF-15

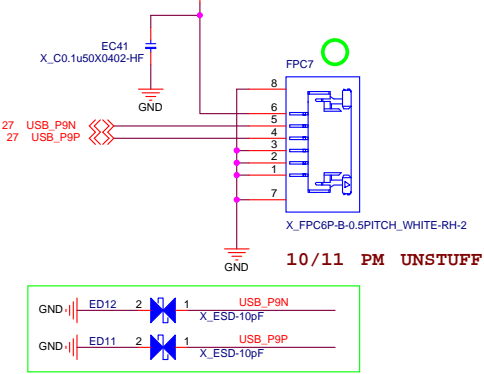
Touch Pad



Same Side



Finger Print 不用

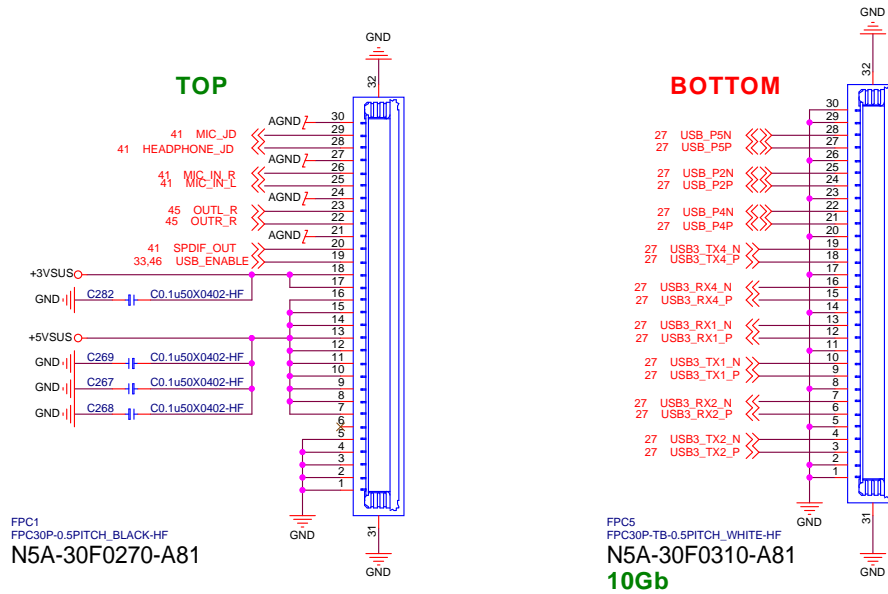


Functional Strap Definitions

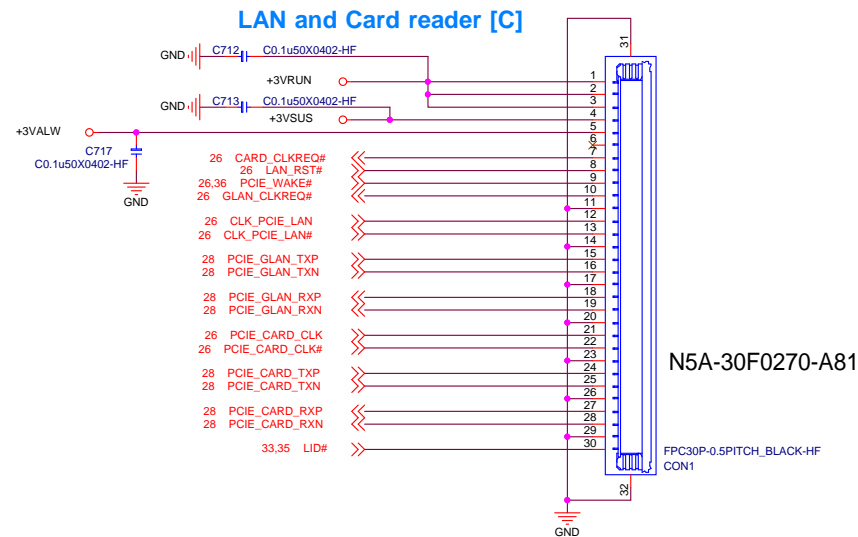
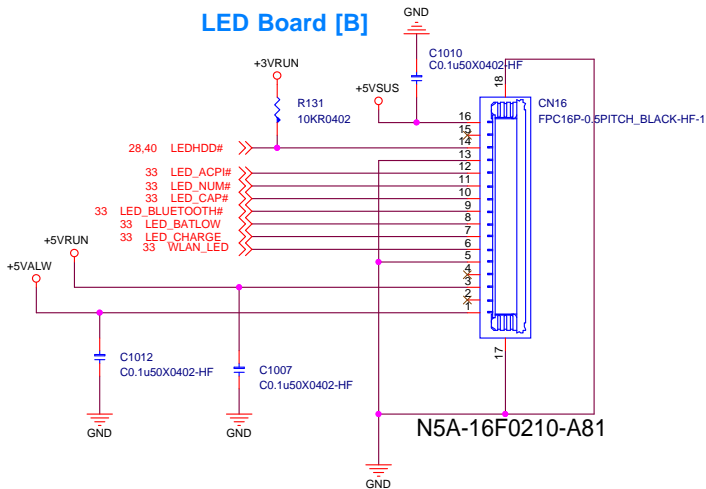
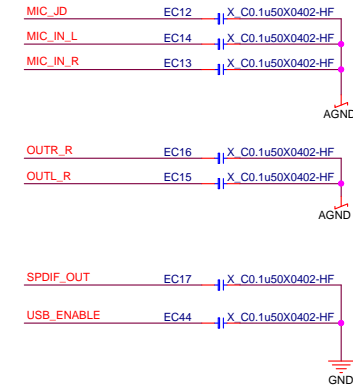
GPP_J4	This signal has a weak internal pull-down. An external pull-up is required on this strap since 38.4 MHz XTAL is not supported on the PCH. 0 = 38.4 MHz XTAL frequency selected. (Default) 1 = 24MHz XTAL frequency selected.
GPP_J6	An external pull-up or pull-down is required. 0 = Integrated CNVi enable. 1 = Integrated CNVi disable.

16K5 BTB CONN (Audio CONN/USB3.0)

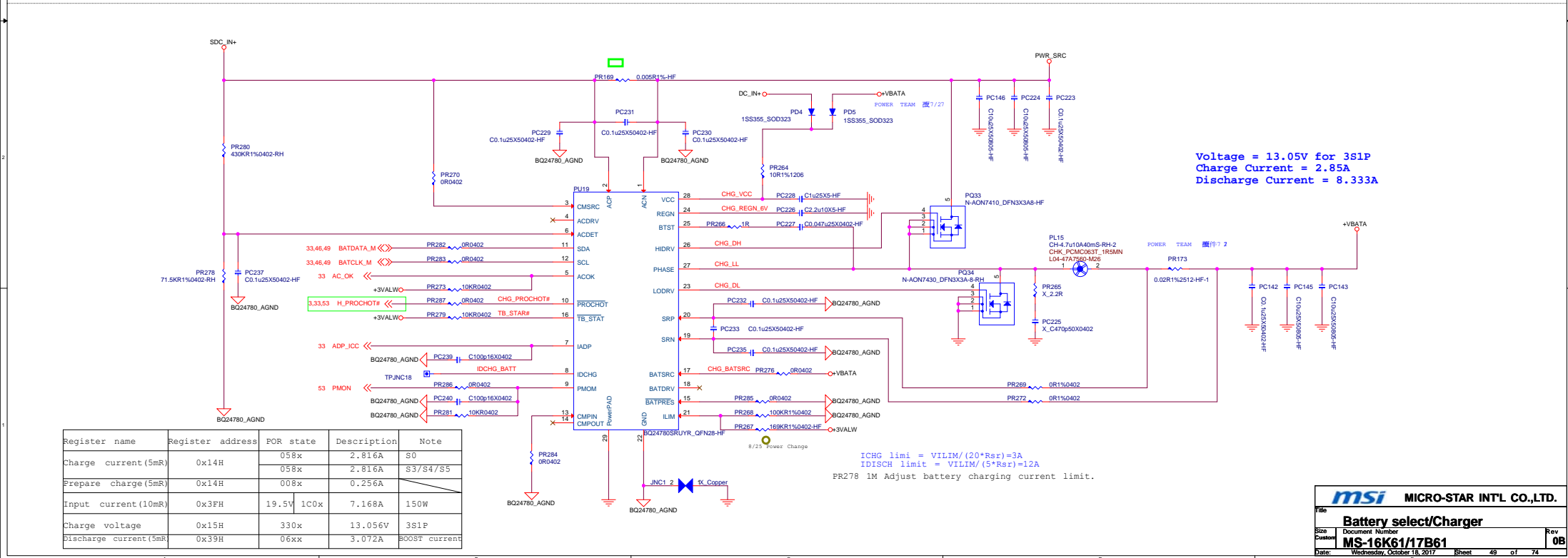
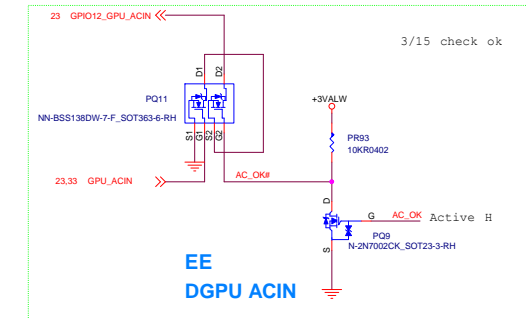
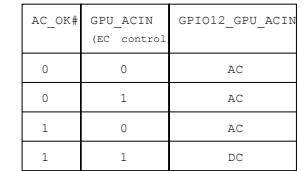
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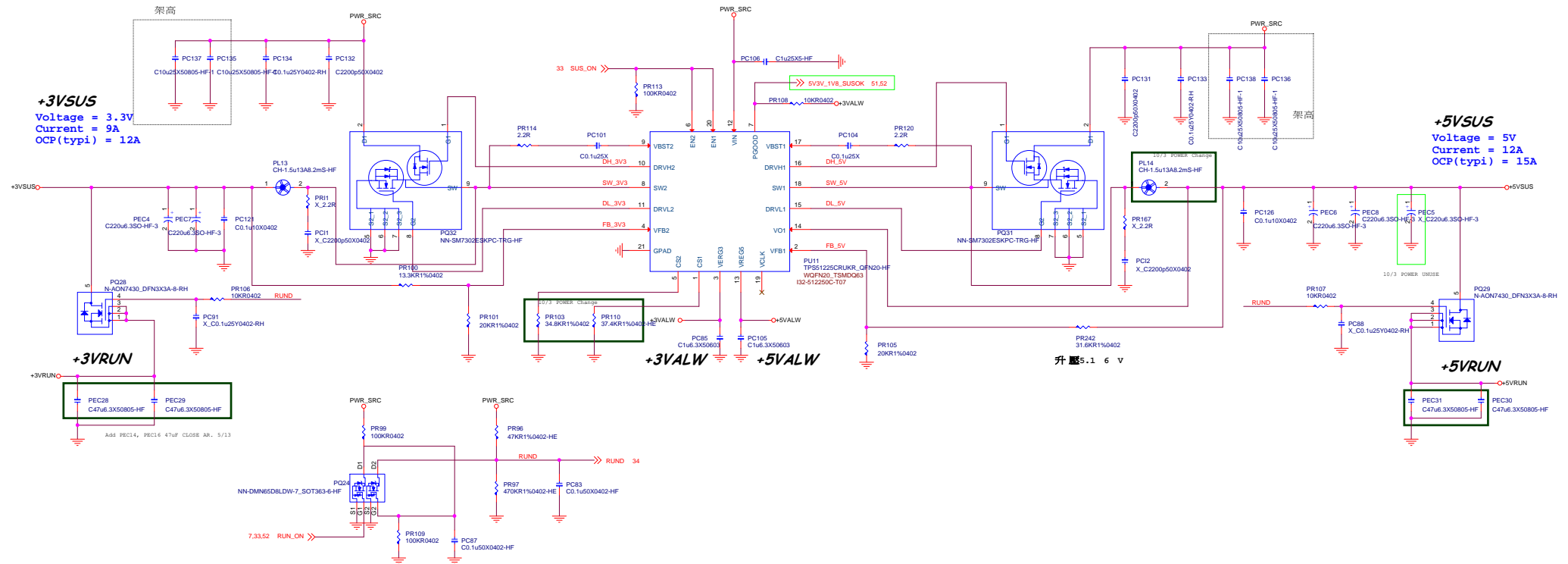


N54-03F0751-S56
9.5A/20V



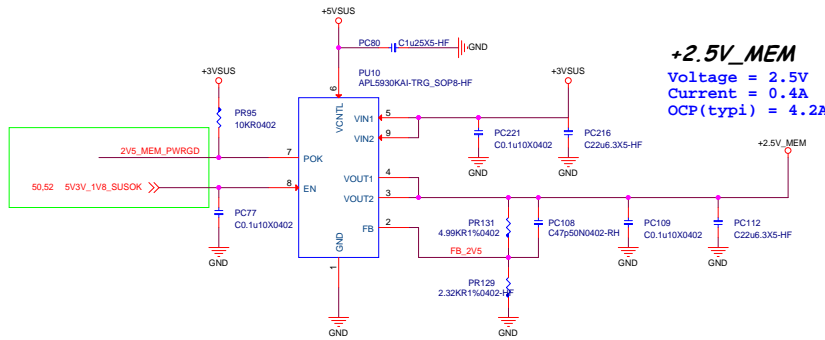
Register name	Register address	POR state	Description	Note
Charge current (5mR)	0x14H	058x	2.816A	S0
		058x	2.816A	S3/S4/S5
Prepare charge (5mR)	0x14H	008x	0.256A	
Input current (10mR)	0x3FH	19.5V	1C0x	7.168A
				150W
Charge voltage	0x15H	330x	13.056V	3S1P
Discharge current (5mR)	0x39H	606xx	3.072A	BOOST current

System Power



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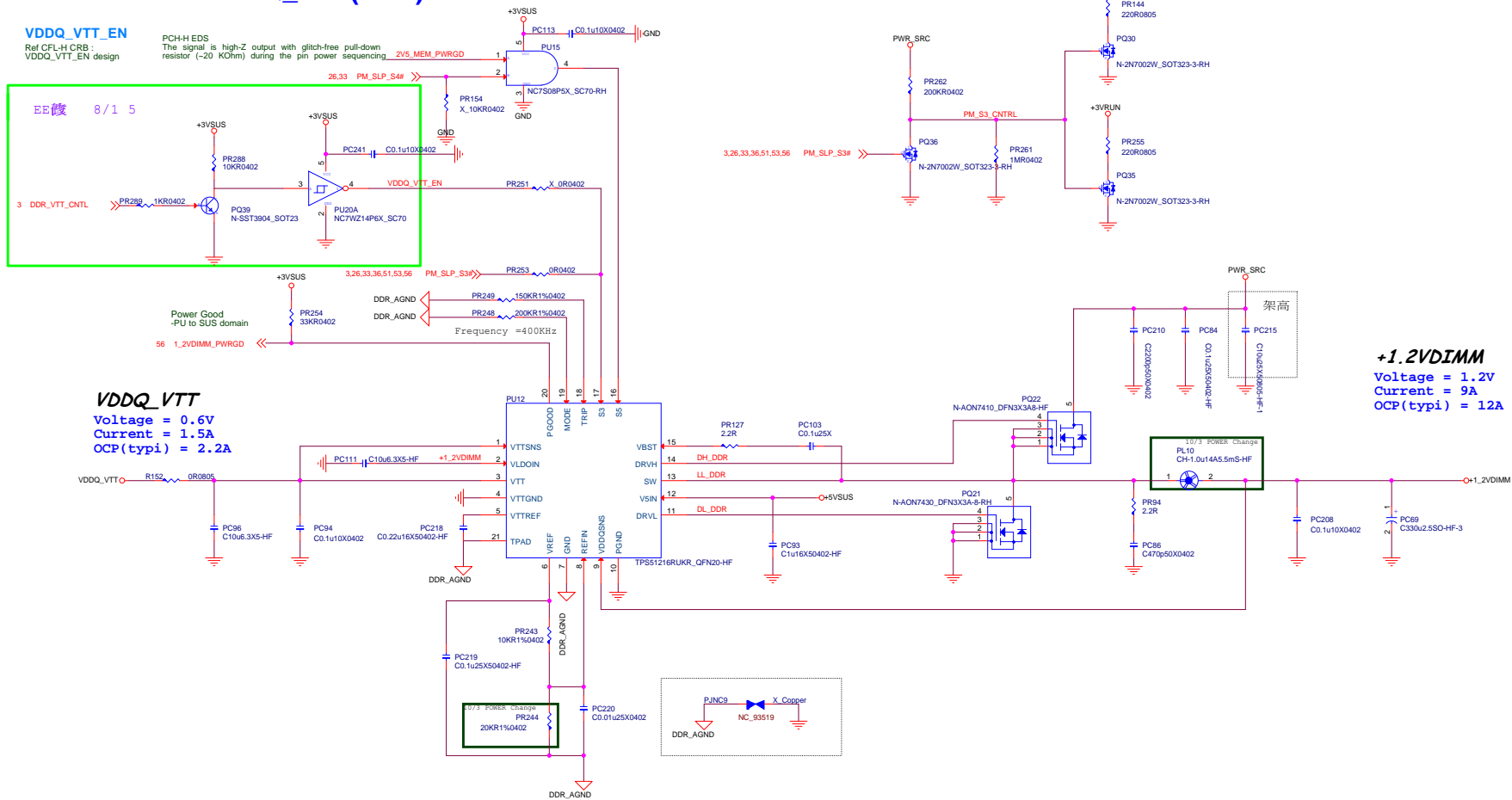
+2.5V_MEM
Voltage = 2.5V
Current = 0.4A
OCP(typi) = 4.2A



VDDQ_VTT_EN
Ref CFL-H CRB :
VDDQ_VTT_EN design

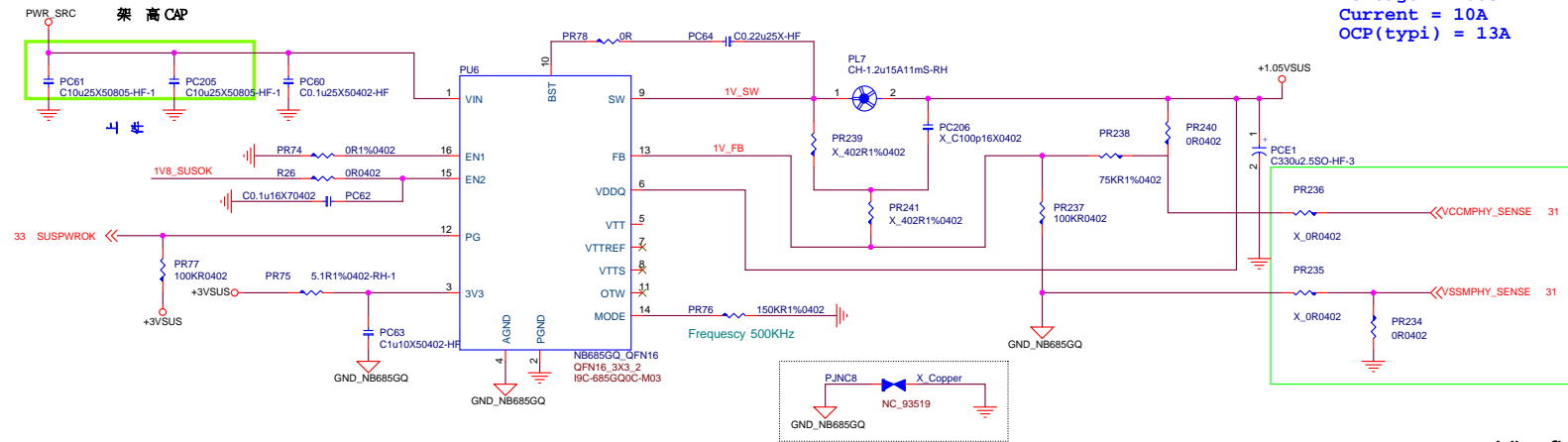
Ref CFL-H CRB :
VDDQ_VTT_EN design

PCH-H EDS
The signal is high-Z output with glitch-free pull-down resistor (~20 KOhm) during the pin power sequencing



+1.2V DIMM
Voltage = 1.2V
Current = 9A
OCP(typ1) = 12A

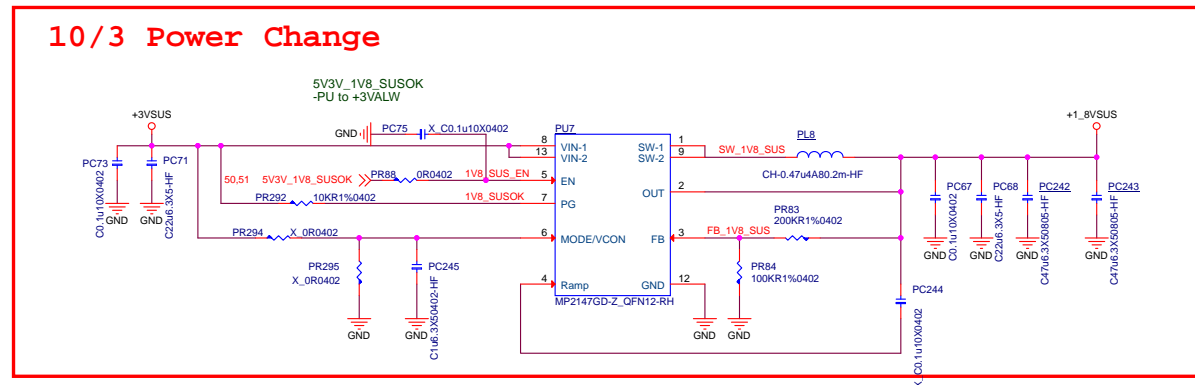
+1.05VSUS



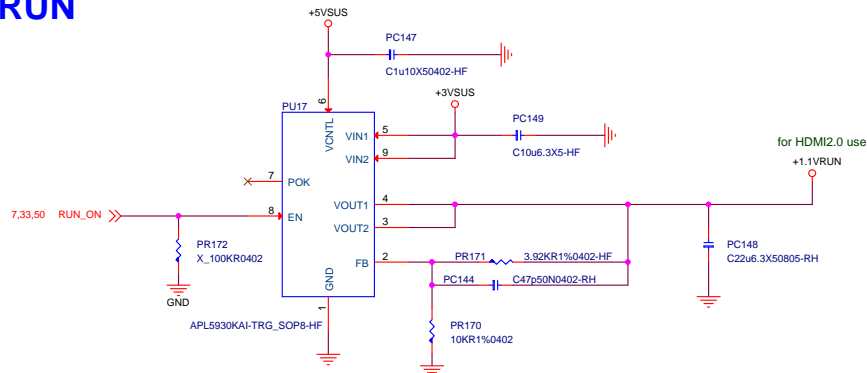
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+1_8VSUS

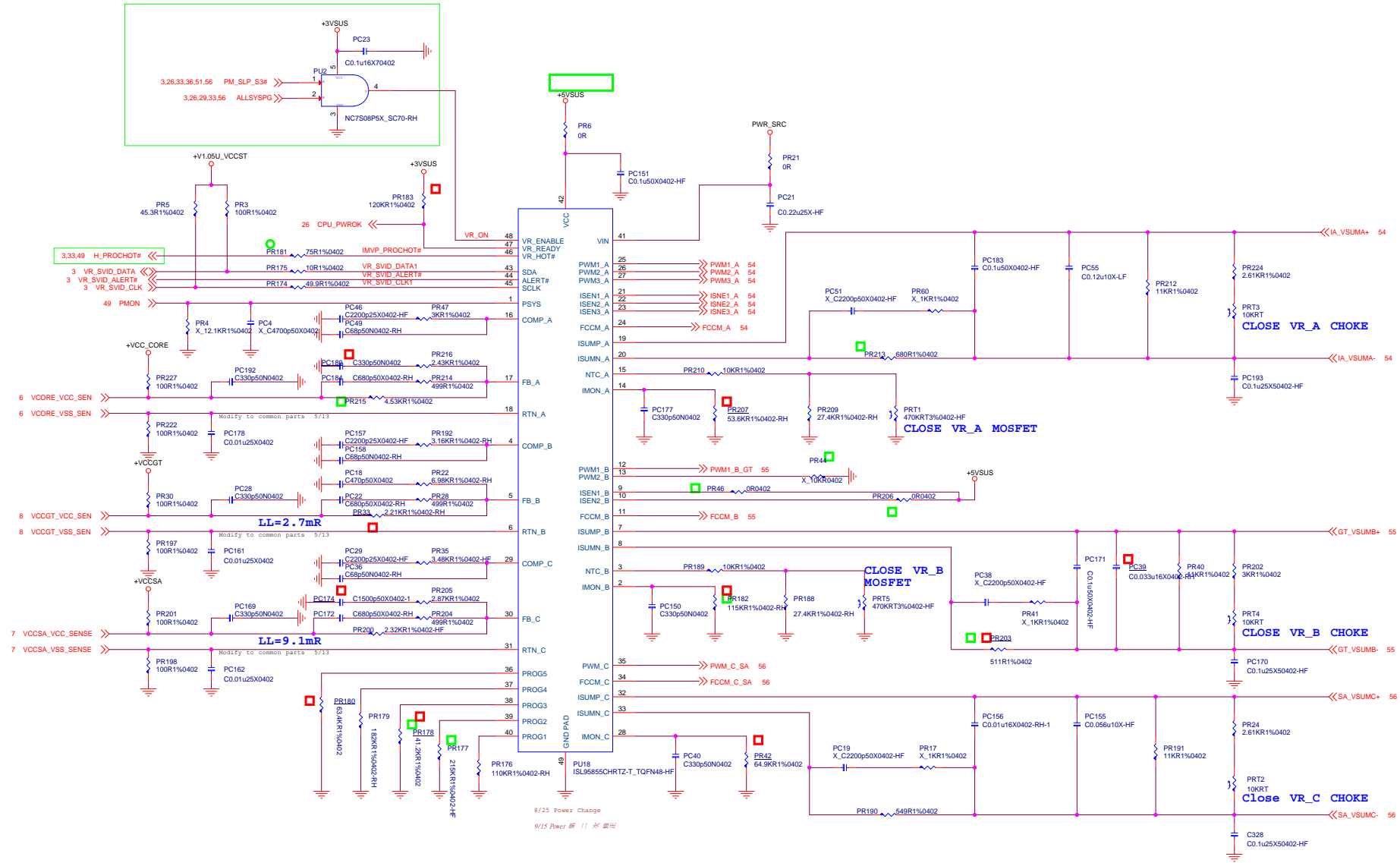
Voltage = 1.8V
Current = 4A
OCF(typi) = 7A



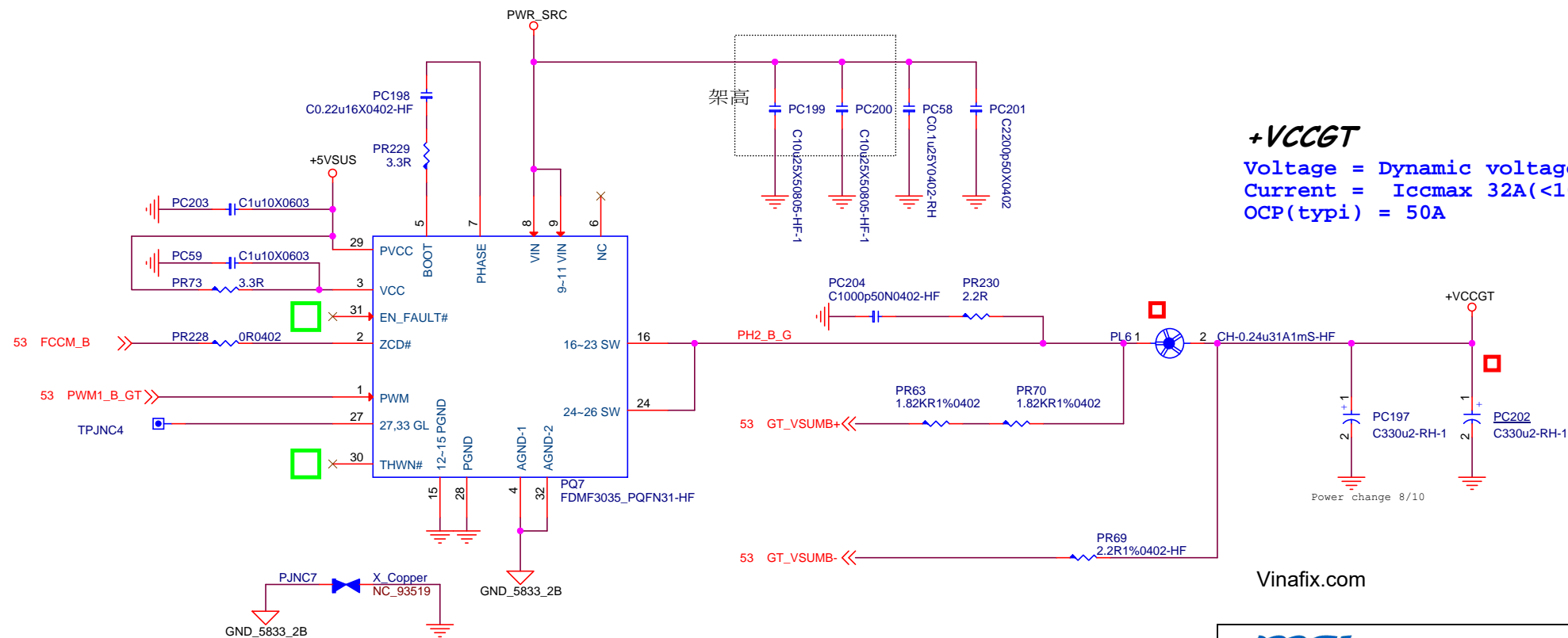
+1.1VRUN




Coffee Lake H-line 6+2 45W ISL95855C



+VCCGT

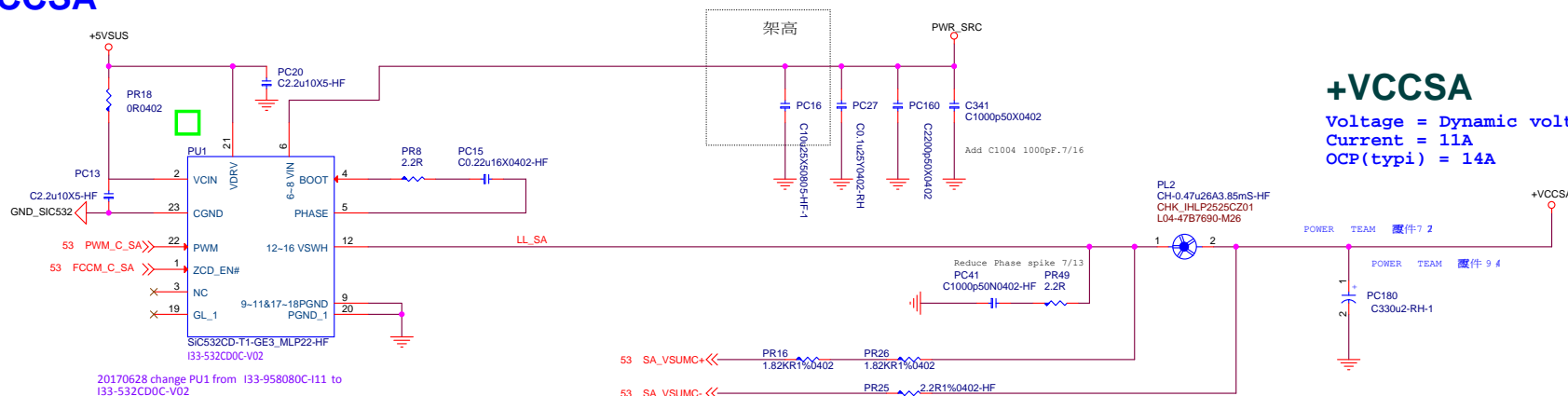


		MICRO-STAR INT'L CO.,LTD.	
Title			
VCCGT			
Size	Document Number		Rev
Custom	MS-16K61/17B61		0B
Date:	Wednesday, October 18, 2017	Sheet 55 of 74	

+VCCSA

+VCCSA

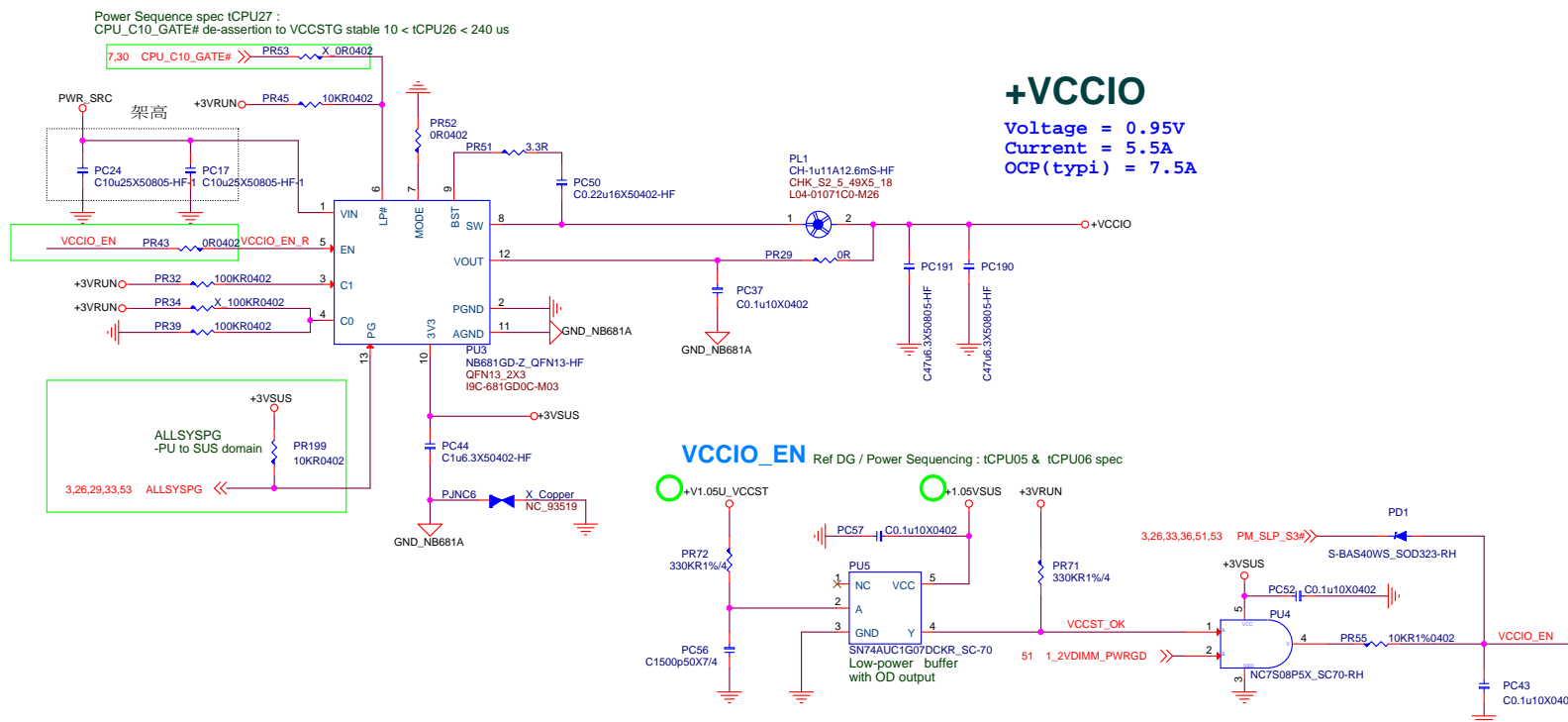
Voltage = Dynamic voltage
Current = 11A
OCP(typi) = 14A



+VCCIO

+VCCIO

Voltage = 0.95V
Current = 5.5A
OCP(typi) = 7.5A



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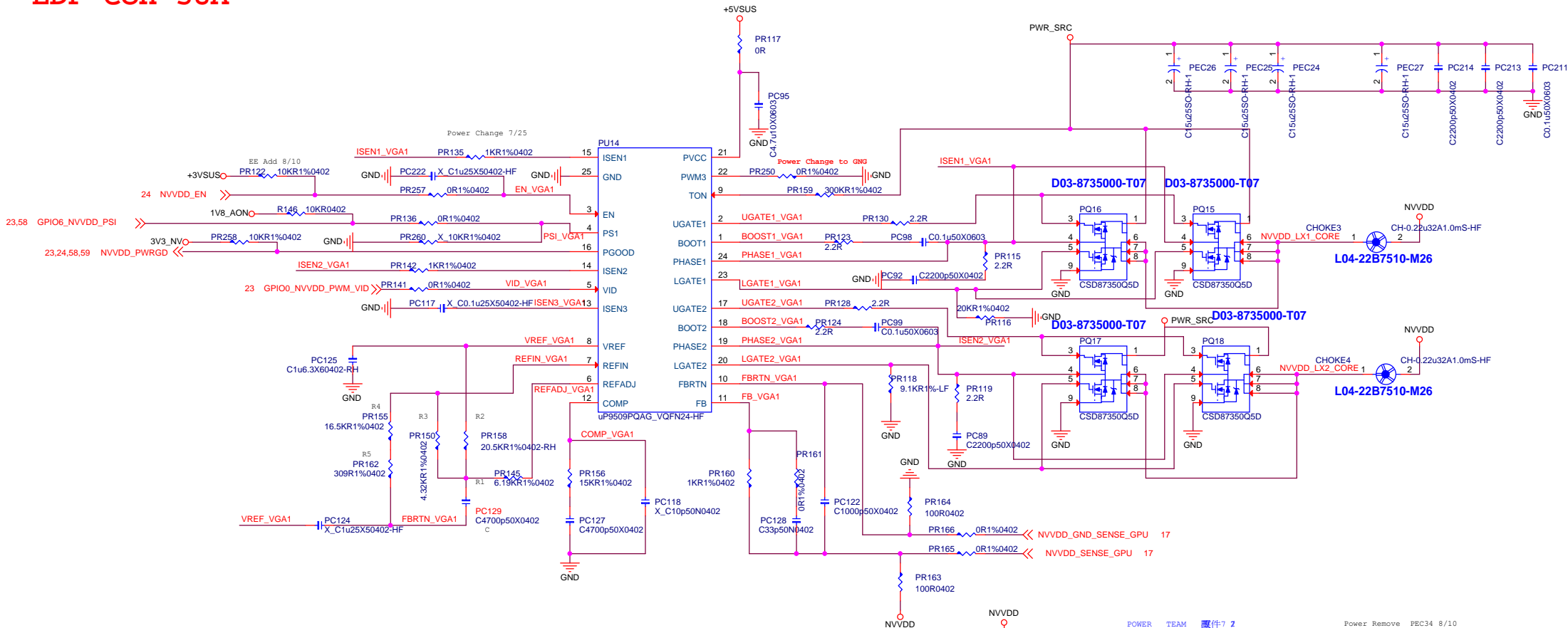
msi MICRO-STAR INT'L CO.,LTD.	
Title	
VCCSA/VCCIO	
Size	Document Number
Custom	MS-16K61/17B61
Date	Wednesday, October 18, 2017
Sheet	56 of 74
Rev	0B

DGPU POWER / UP9509P

EDP-Peak 136A
EDP-Con 58A

DGPU POWER NVVDD

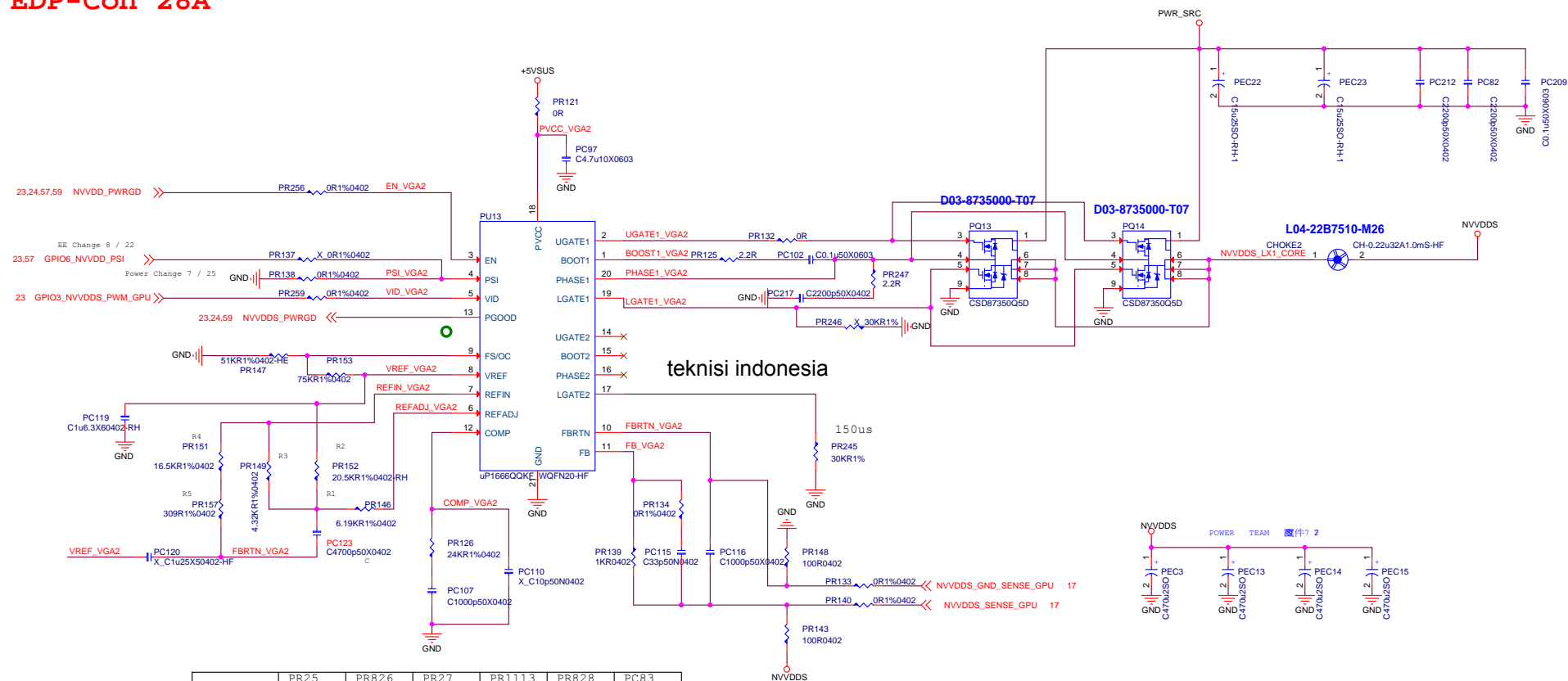
VBoot:0.8V
Vmin:0.3V / Vmax:1.3V



	PR145	PR158	PR150	PR155	PR162	PC129
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

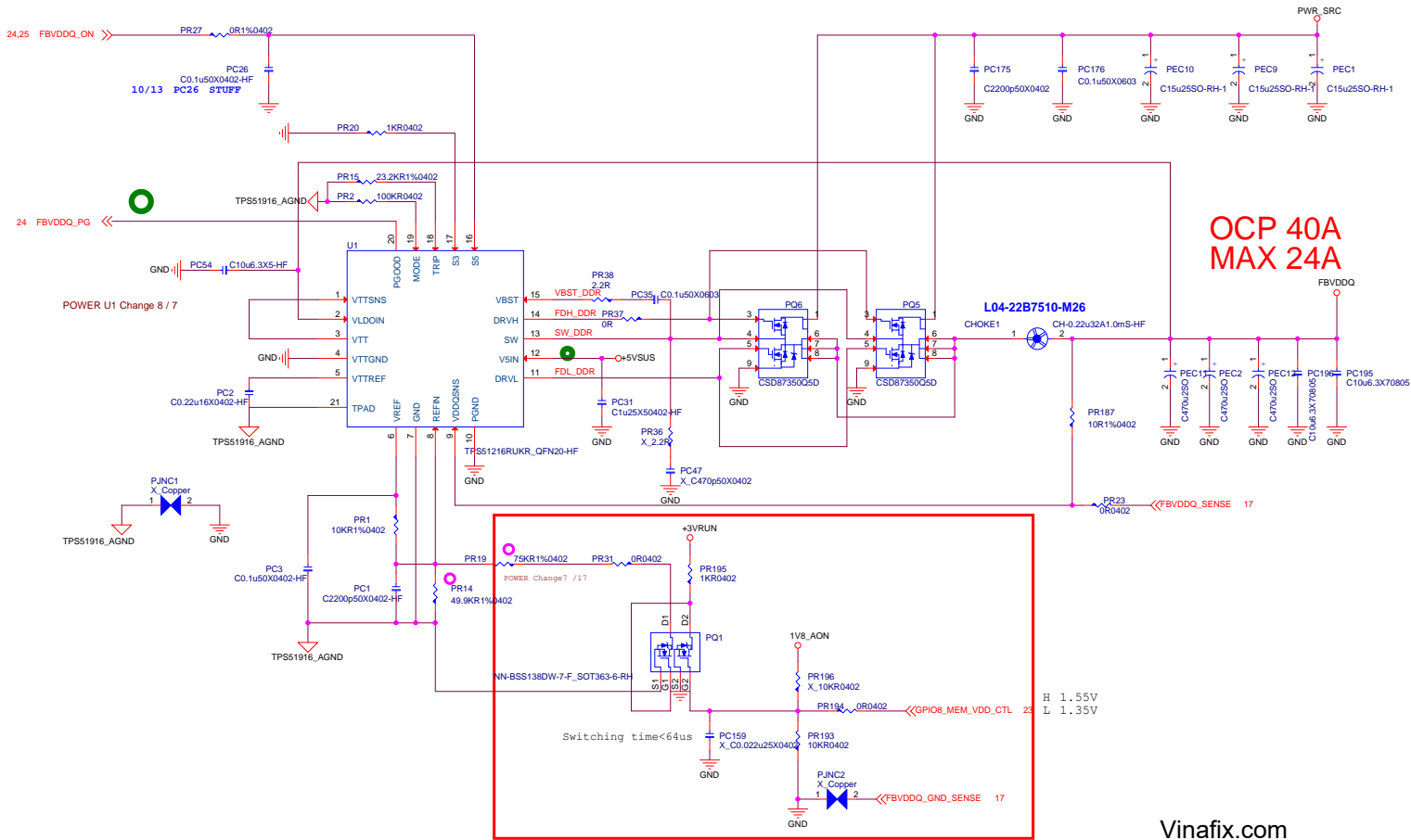
EDP-Peak 74A
EDP-Con 28A

VBoot:0.8V
Vmin:0.3V / Vmax:1.3V

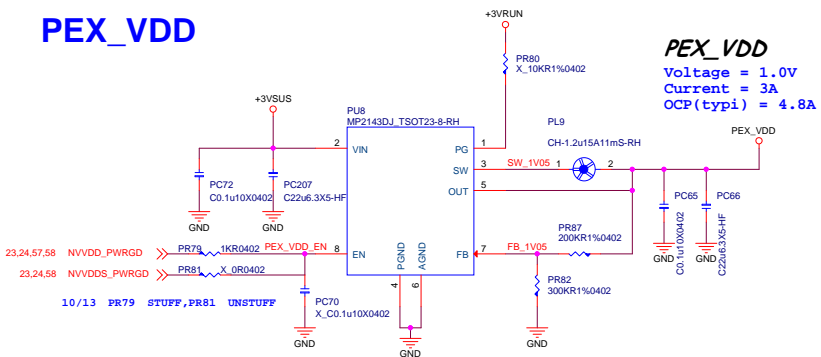


	PR25	PR826	PR27	PR1113	PR828	PC83
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	1.5nF

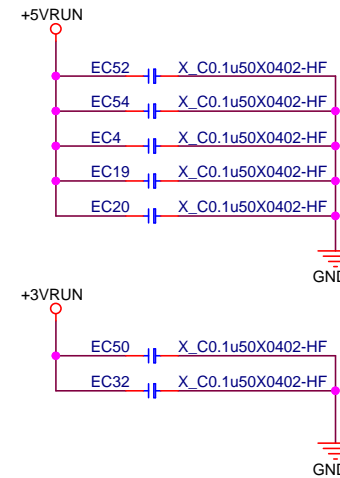
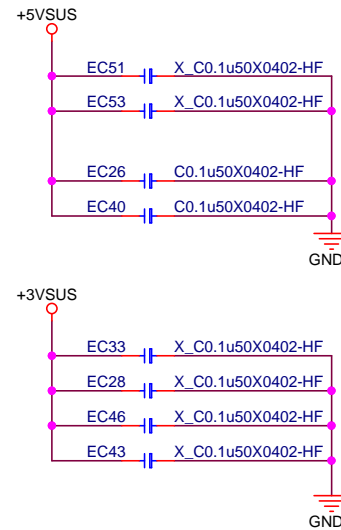
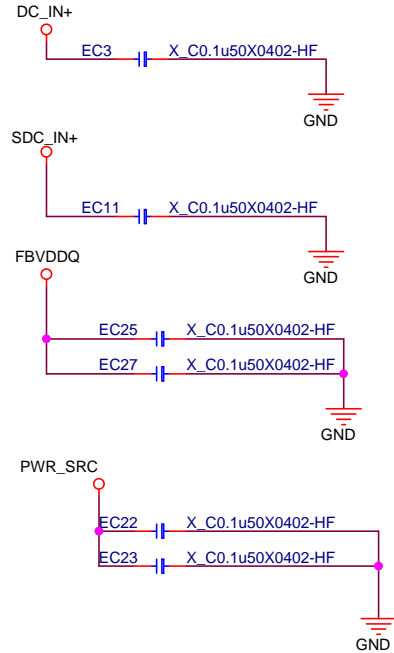
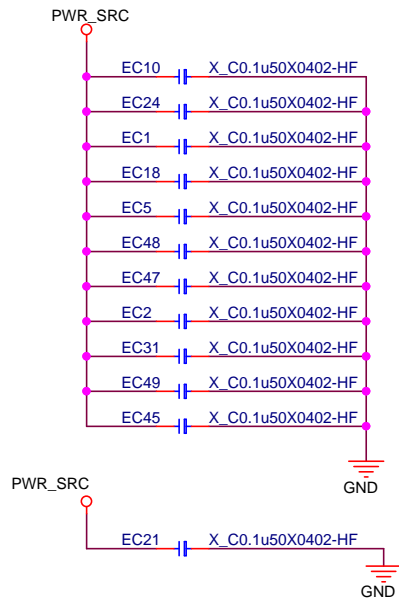
FBVDDQ



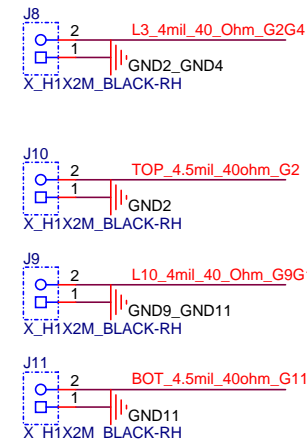
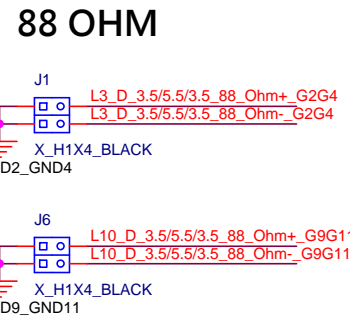
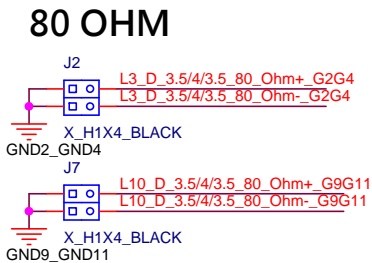
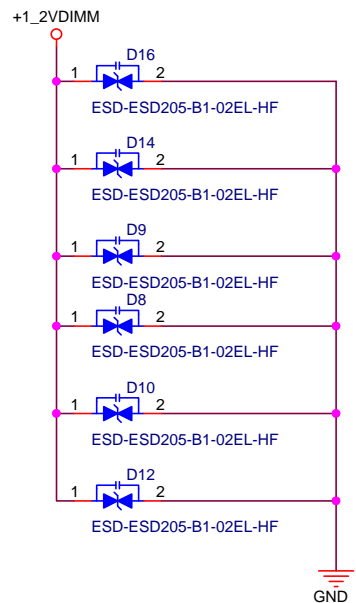
PEX_VDD




EMI

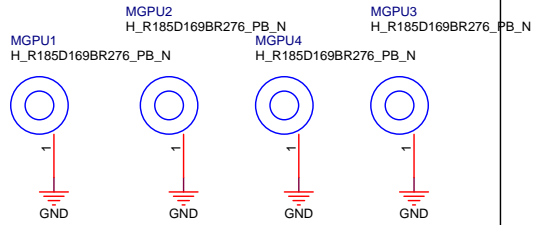


40 OHM

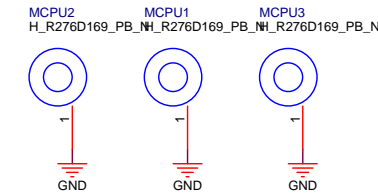


		MICRO-STAR INT'L CO.,LTD.	
Title			
EMI			
Size	Document Number		Rev
Custom	MS-16K61/17B61		0
Date:	Wednesday, October 18, 2017	Sheet	60 of 74

dGPU Holes



CPU Holes



CPU BKT

CPU BRACKET
307-6K50111-A89

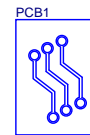
MB
MYLAR

X_MB_mylar
E2P-3F11111-Y42

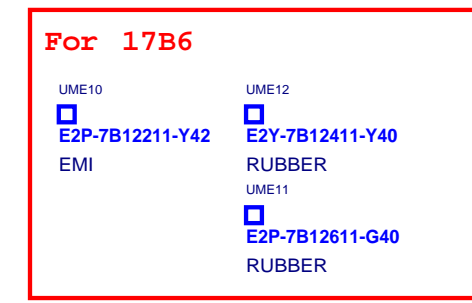
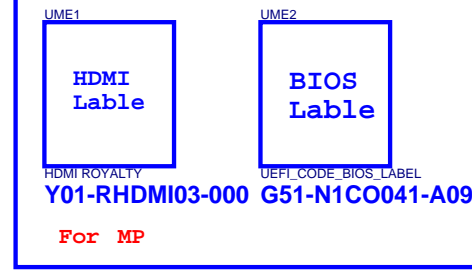
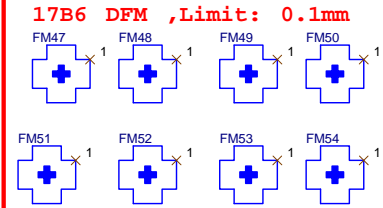
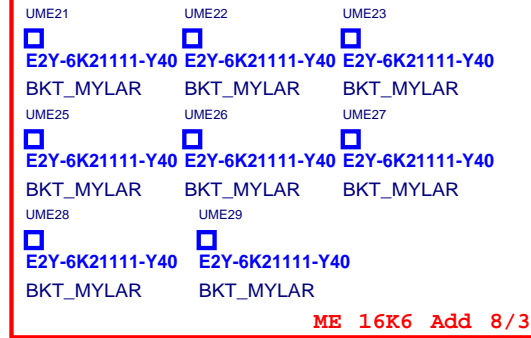
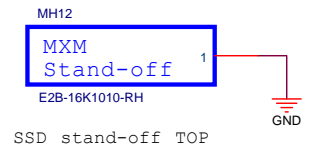
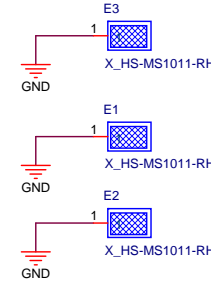
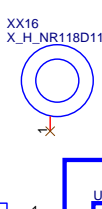
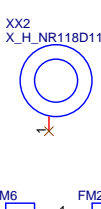
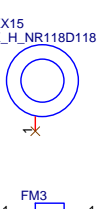
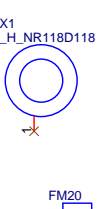
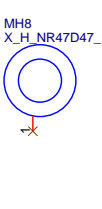
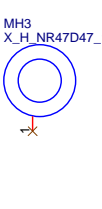
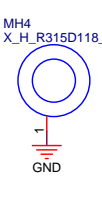
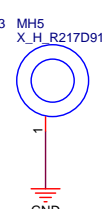
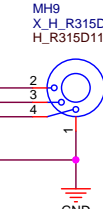
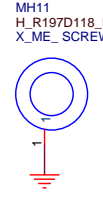
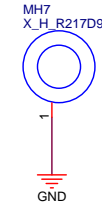
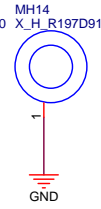
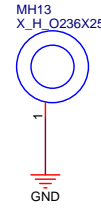
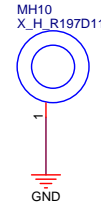
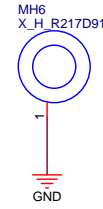
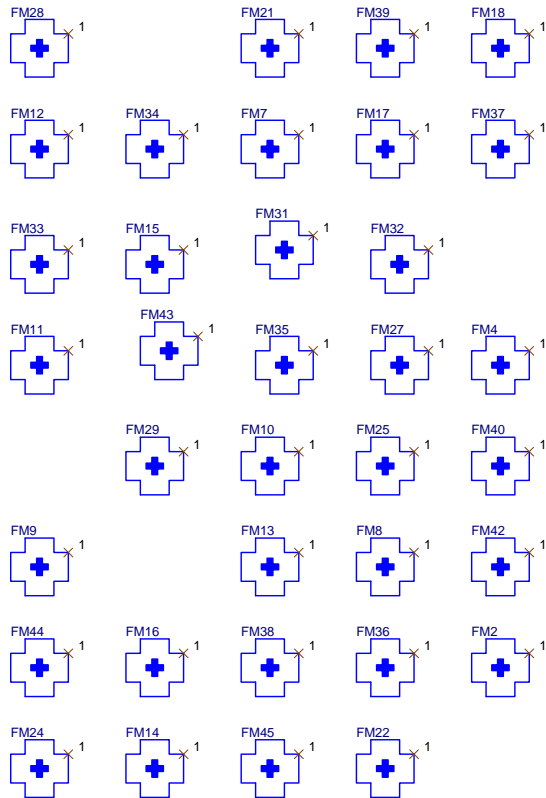
GPU BKT

GPU BRACKET
307-7B10112-Y77

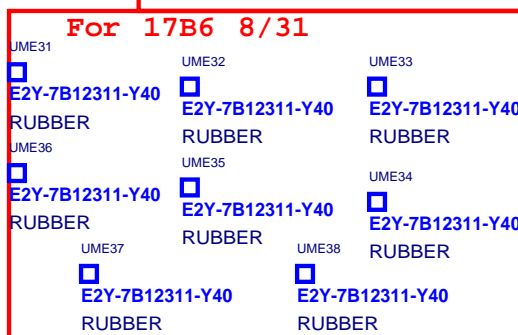
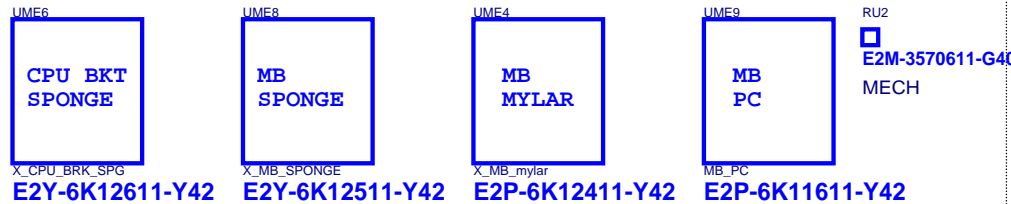
AVL : 7M7-17B112-008



AVL PD0-16K610B-H73
:PD0-16K610B-T53



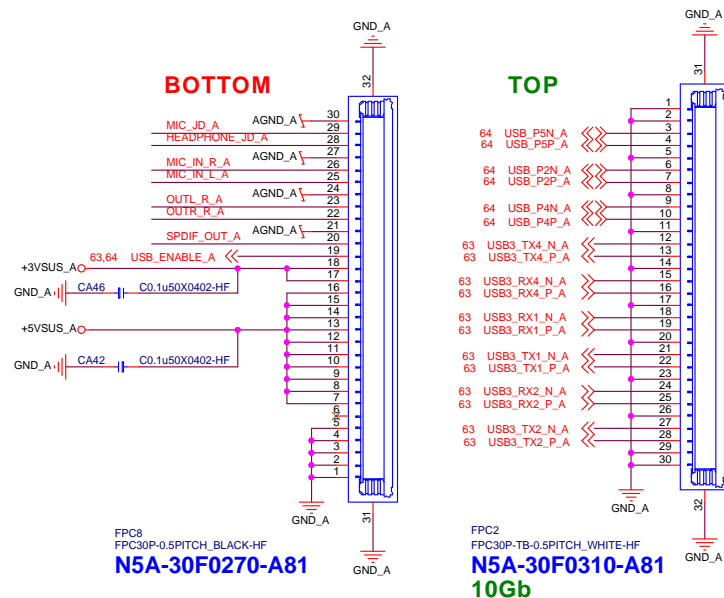
For 16K2



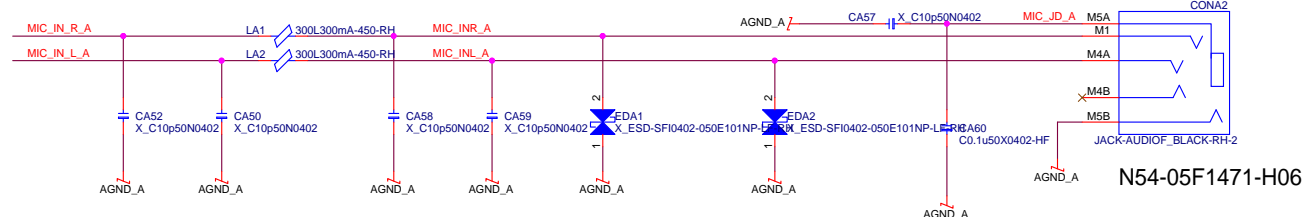
16K5-A Board (Audio CONN)

BTB Connector From MB
CONN Pin Current Capability : ???A/Pin

HP OUT / SPDIF OUT

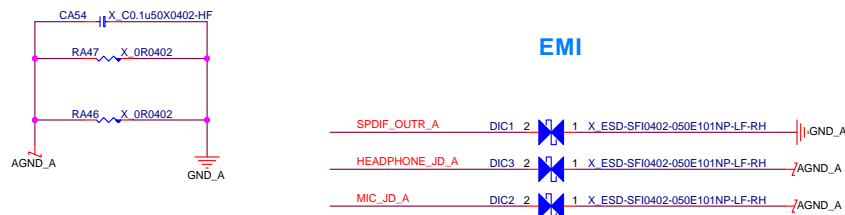


MIC IN

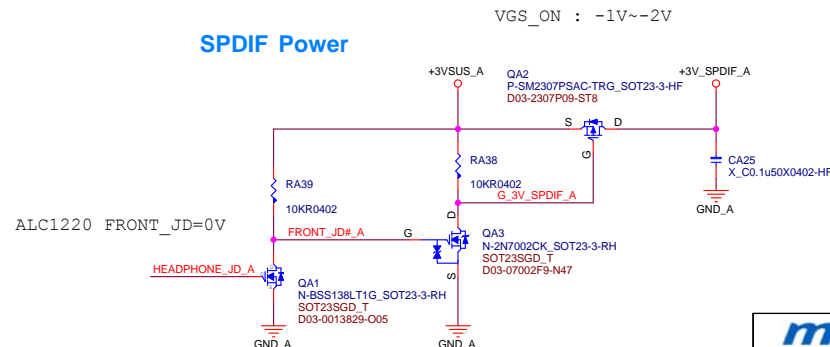


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EMI



SPDIF Power



USB3.1 Gne2 Redriver

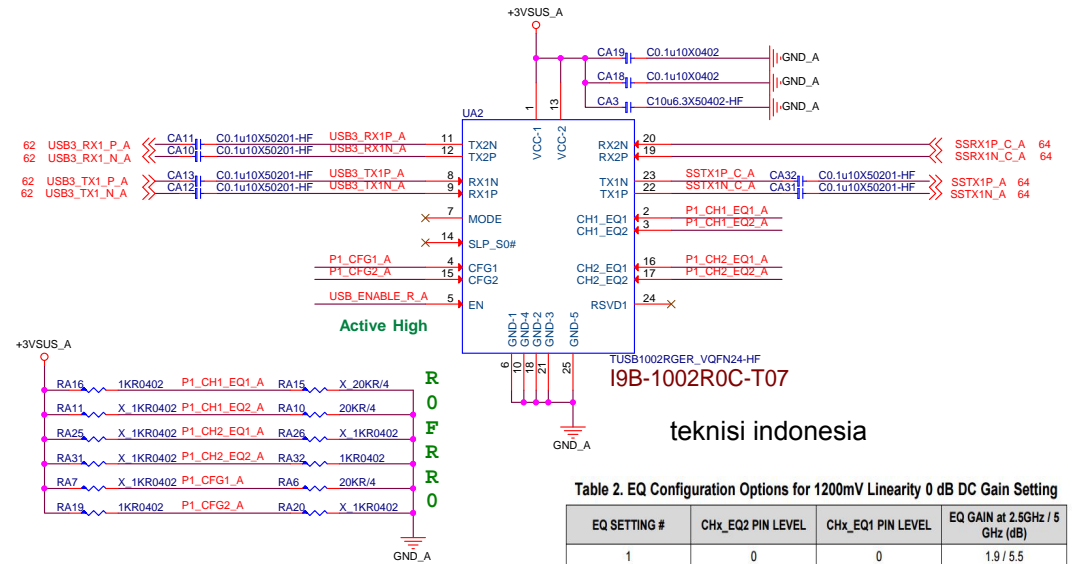
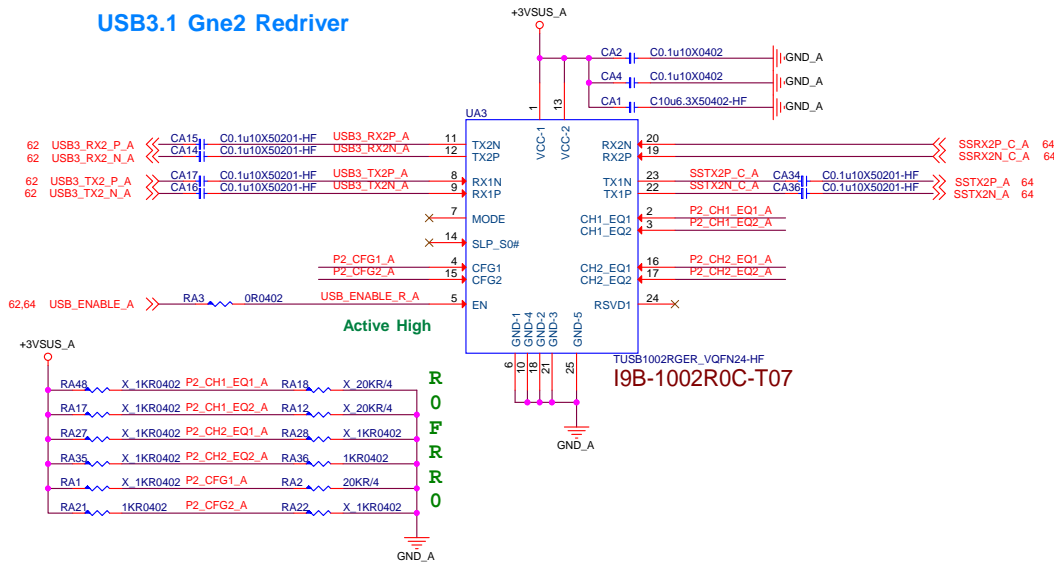


Table 2. EQ Configuration Options for 1200mV Linearity 0 dB DC Gain Setting

EQ SETTING #	CHX_EQ2 PIN LEVEL	CHX_EQ1 PIN LEVEL	EQ GAIN at 2.5GHz / 5 GHz (dB)
1	0	0	1.9 / 5.5
2	0	R	2.8 / 7.1
3	0	F	3.5 / 8.2
4	0	1	4.4 / 9.3
5	R	0	5.0 / 10.2
6	R	R	5.8 / 11.1
7	R	F	6.4 / 11.8
8	R	1	7.1 / 12.6
9	F	0	7.6 / 13.1
10	F	R	8.2 / 13.8
11	F	F	8.7 / 14.3
12	F	1	9.2 / 14.8
13	1	0	9.6 / 15.2
14	1	R	10.1 / 15.6
15	1	F	Reserved.
16	1	1	Reserved.

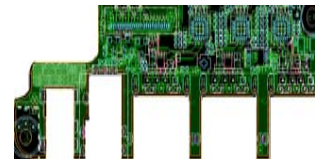
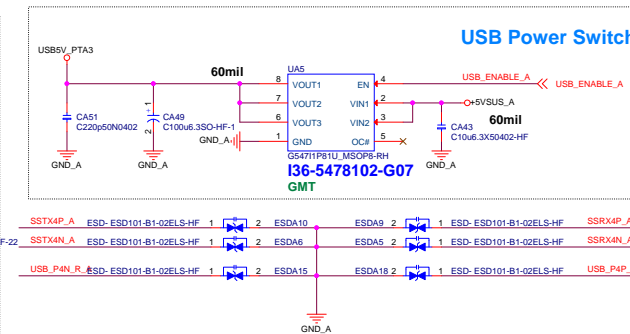
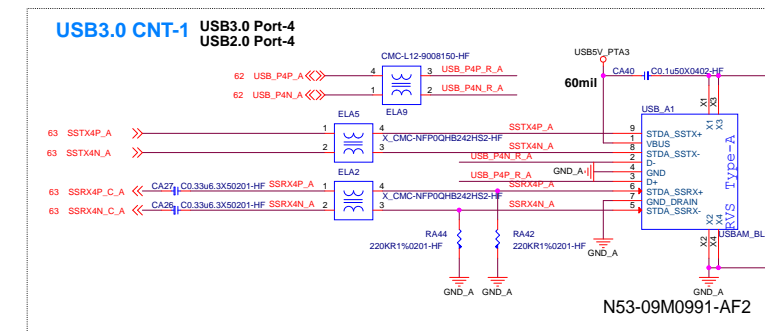
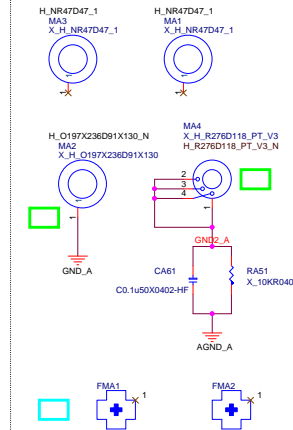
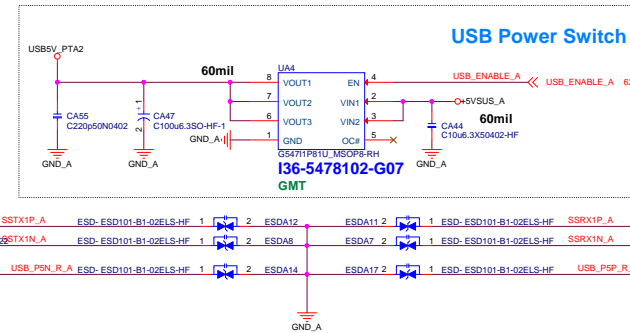
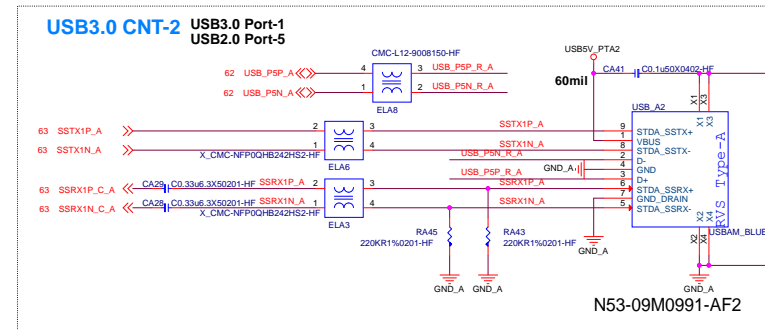
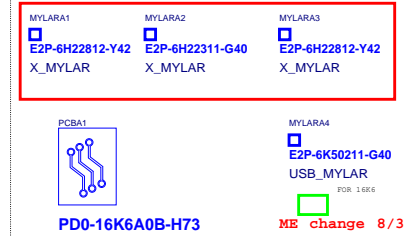
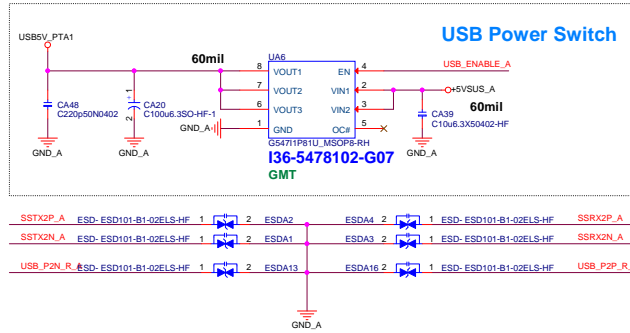
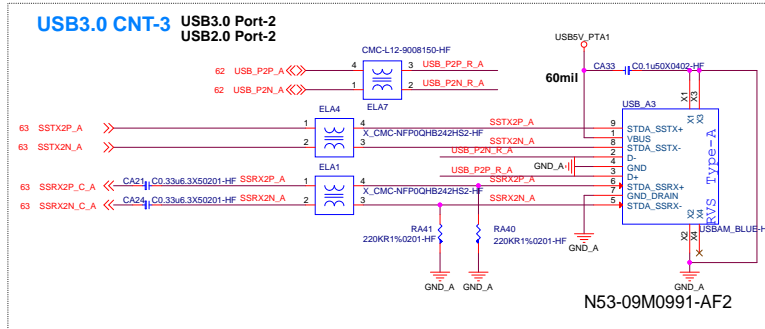
Table 3. VOD Linear Range and DC Gain

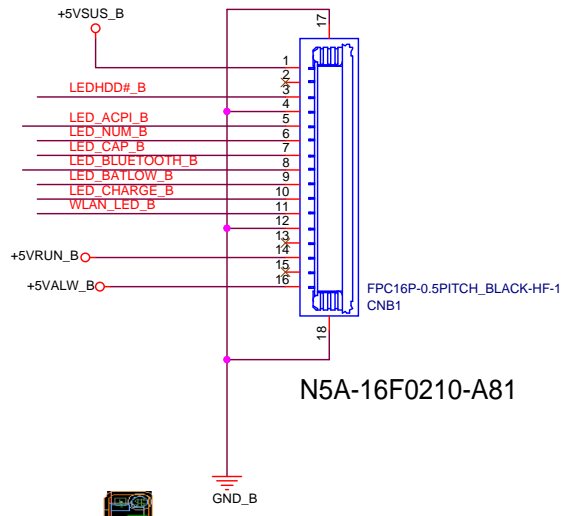
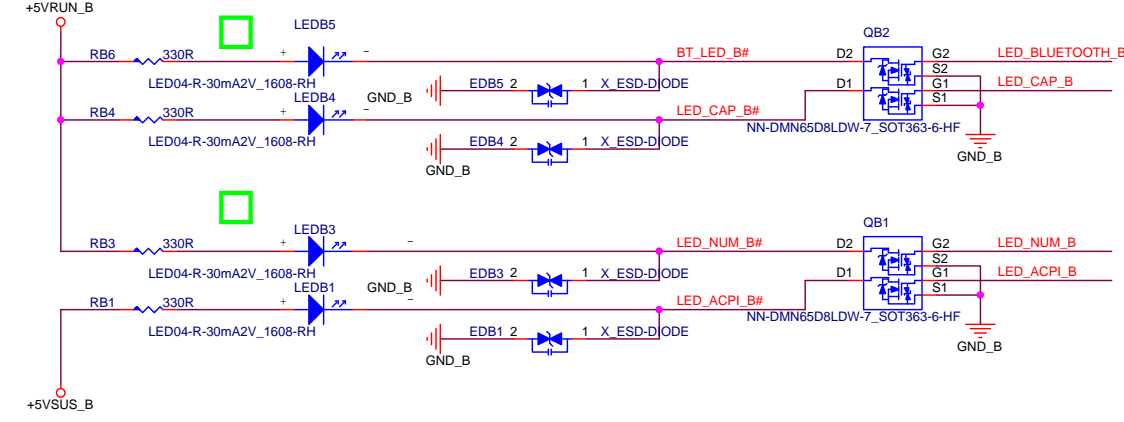
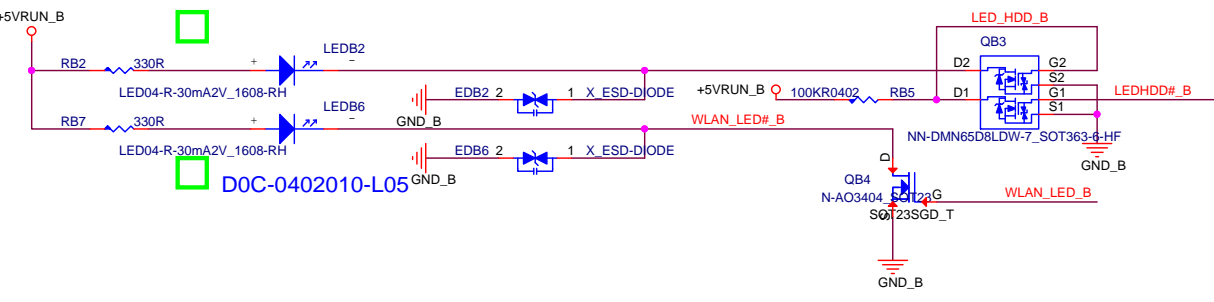
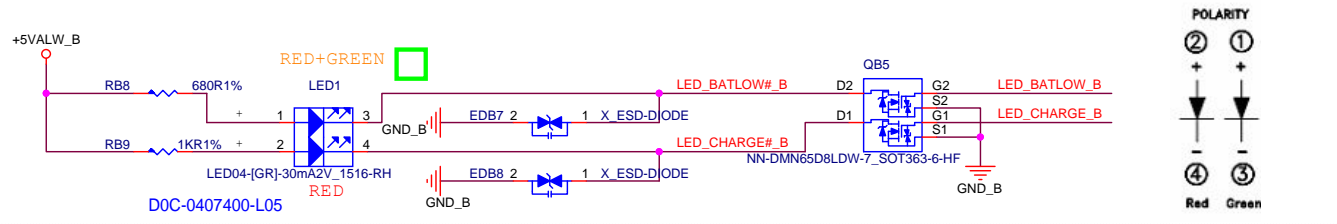
SETTING #	CFG1 PIN LEVEL	CFG2 PIN LEVEL	CH1 DC GAIN (dB)	CH2 DC GAIN (dB)	CH1 V _{CO} LINEAR RANGE (mVpp)	CH2 V _{CO} LINEAR RANGE (mVpp)
1	0	0	+1	0	900	900
2	0	R	0	+1	900	900
3	0	F	0	0	900	900
4	0	1	+1	+1	900	900
5	R	0	0	0	1000	1000
6	R	R	+1	0	1000	1000
7	R	F	0	-1	1000	1000
8	R	1	+2	+2	1000	1000
9	F	0	-1	-1	1200	1200
10	F	R	-2	-2	1200	1200
11	F	F	0	0	1200	1200
12	F	1	+1	+1	1200	1200
13	1	0	-1	0	1200	1200
14	1	R	0	-1	1200	1200
15	1	F	0	+1	1200	1200
16	1	1	+1	0	1200	1200

Table 1. 4-Level Control Pin Settings

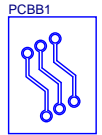
LEVEL	SETTINGS
0	Option 1: Tie 1 K Ω 5% to GND. Option 2: Tie directly to GND.
R	Tie 20 K Ω 5% to GND.
F	Float (leave pin open)
1	Option 1: Tie 1 K Ω 5% to V _{CC} . Option 2: Tie directly to V _{CC} .

[A] USB3.0 CNT-2/-3

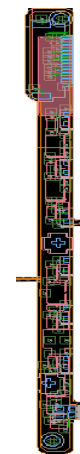
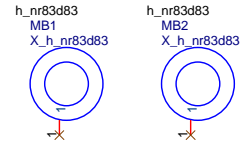
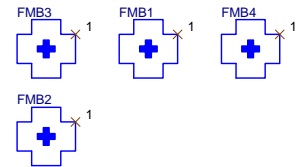





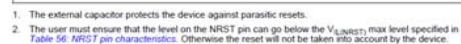
Hannstar: H73
TRIPOD: T53



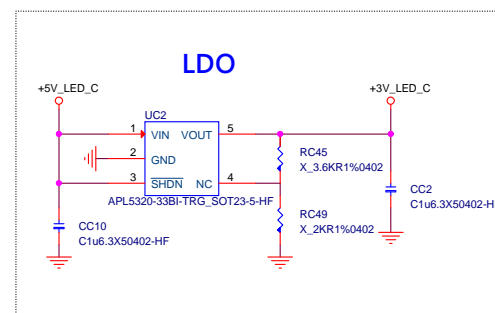
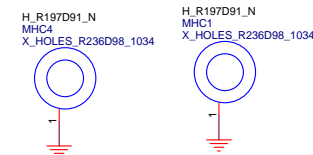
PD0-16K6B0B-H73
AVL : PD0-16K6B0B-T53




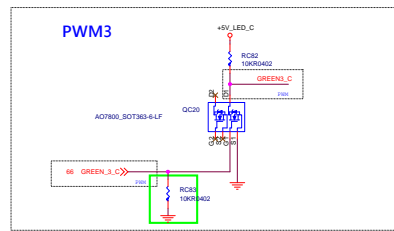
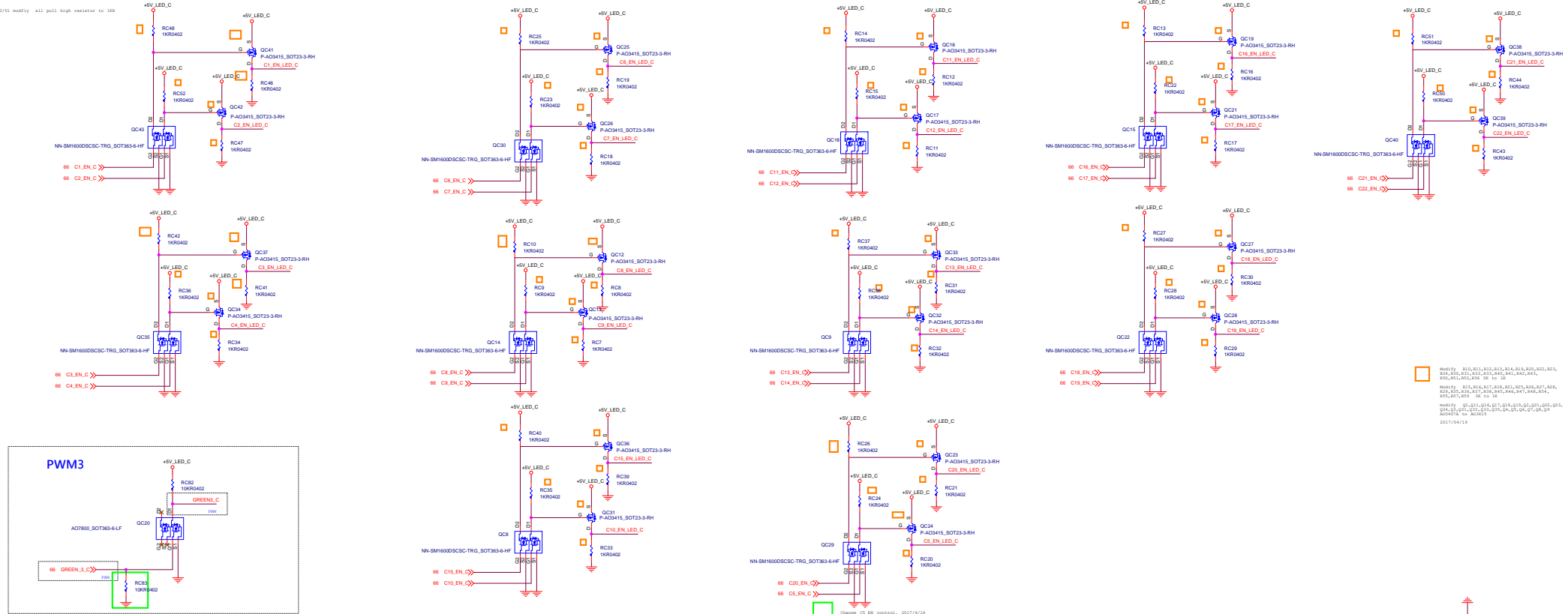
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Title			
[B] LED			
Size	Document Number		Rev
B	MS-16K6B/MS-17B6B		0B
Date:	Wednesday, October 18, 2017	Sheet	65 of 74



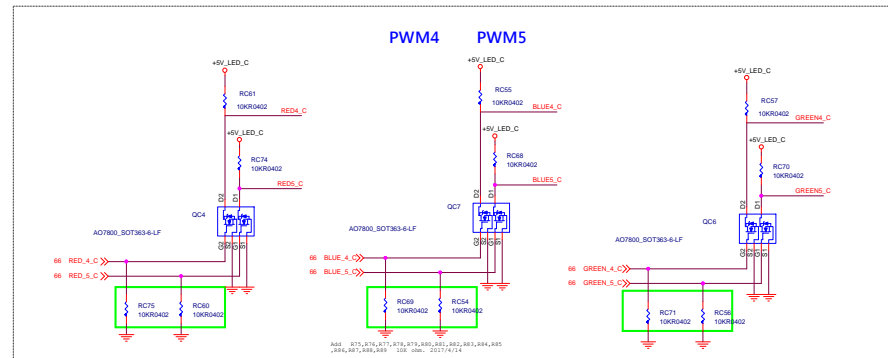
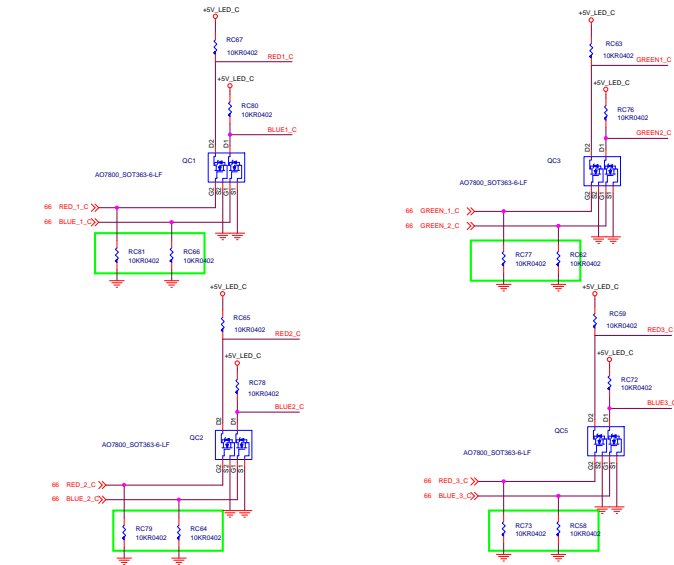
Confirm Pin 1 position



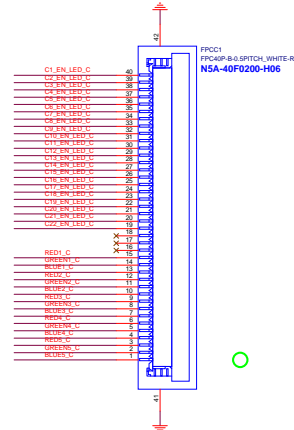
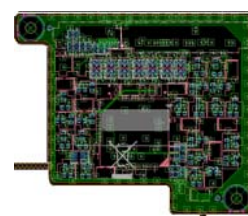
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Title	[C]MCU/Matrix/Power
Size	Document Number MS-16K6C
Date:	Sheet 66 of 74 Rev 0B



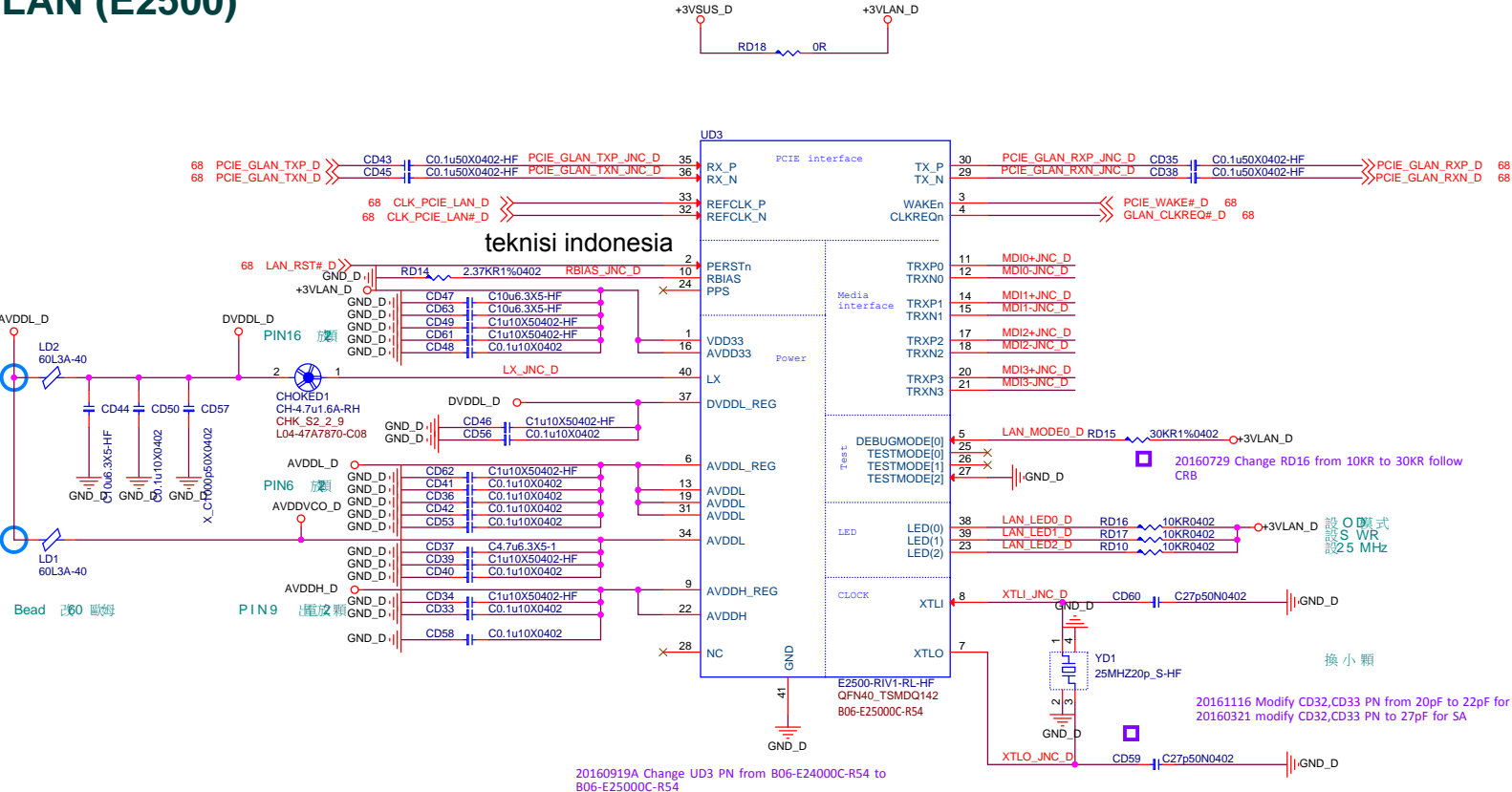
PWM1 PWM2 PWM3



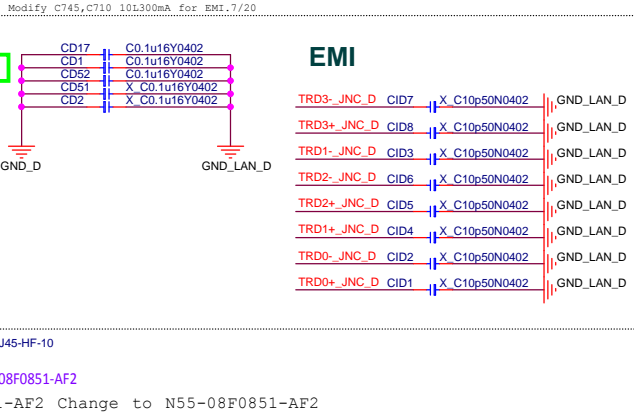
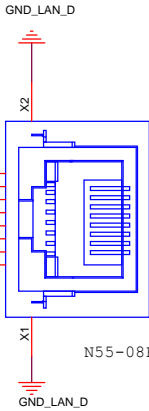
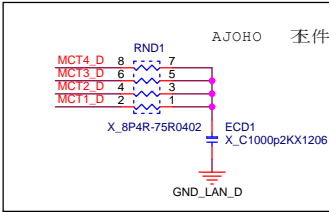
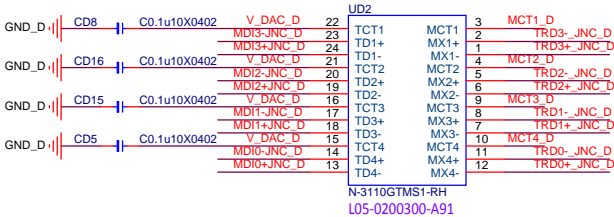
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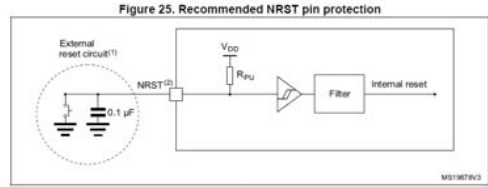
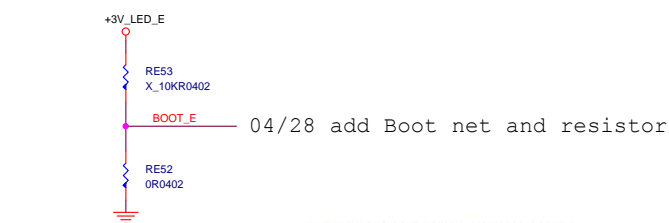
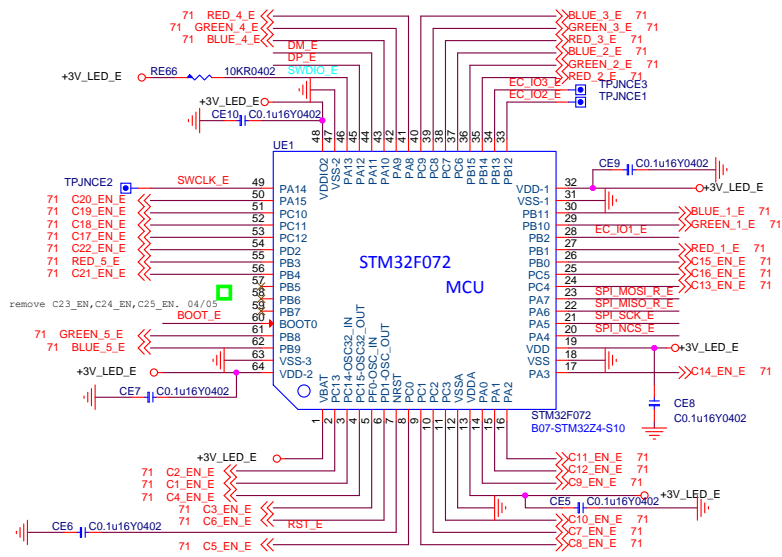


LAN (E2500)

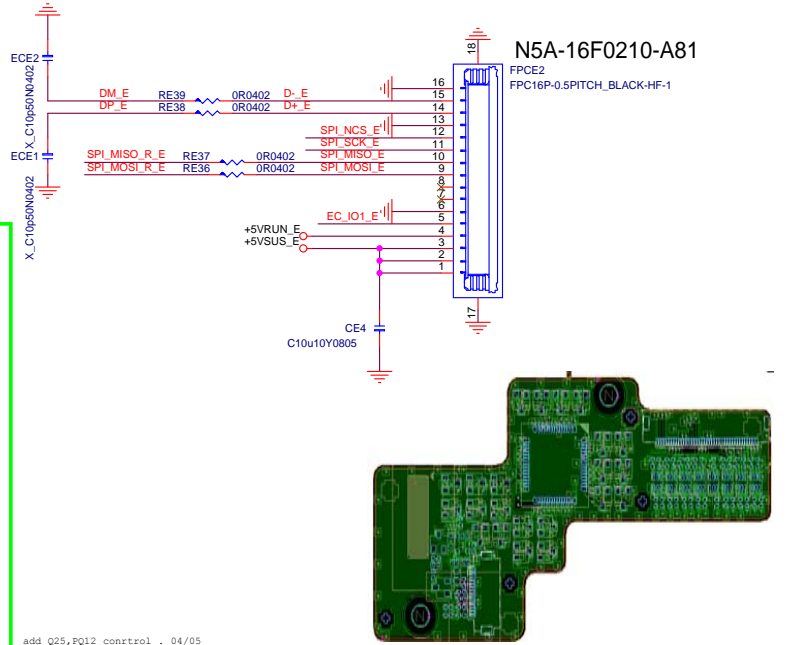
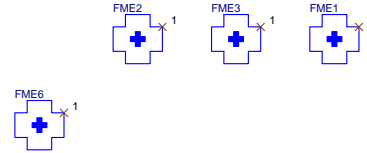
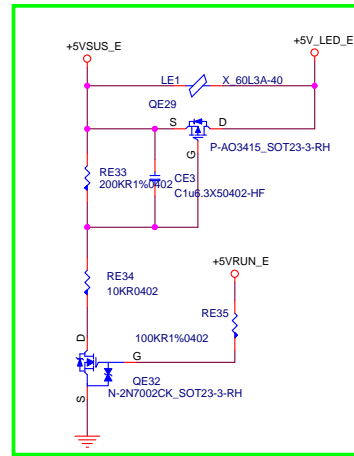


20160729 Delete RD10 10L on MCT1_D net

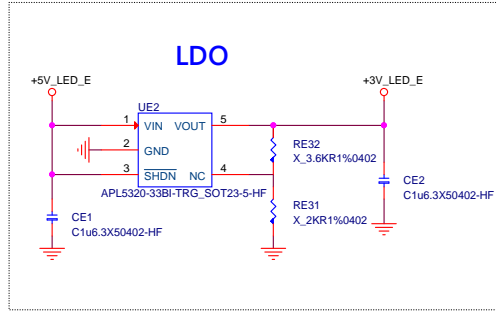
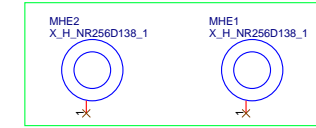
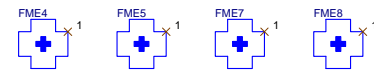




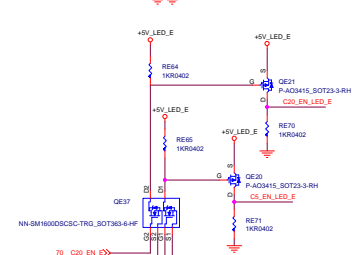
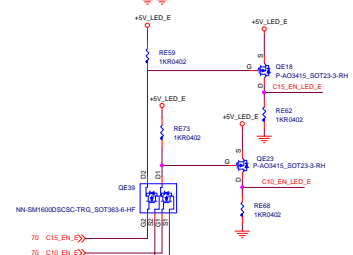
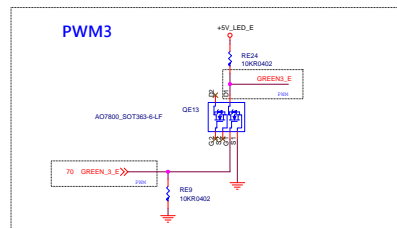
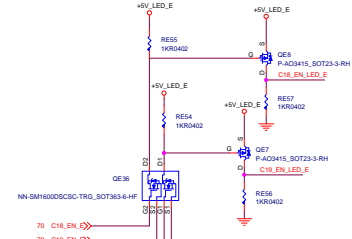
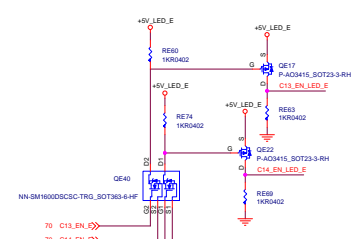
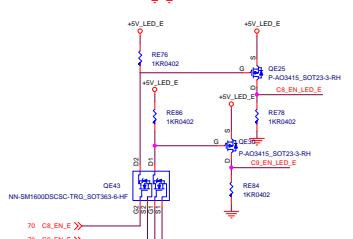
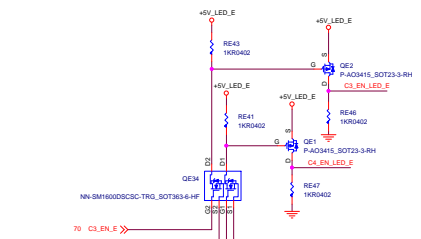
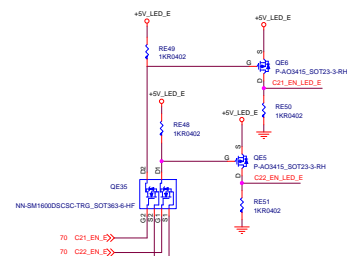
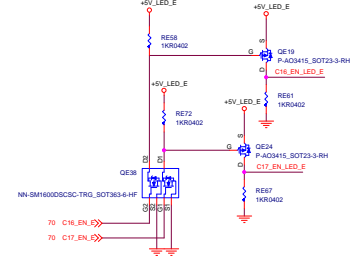
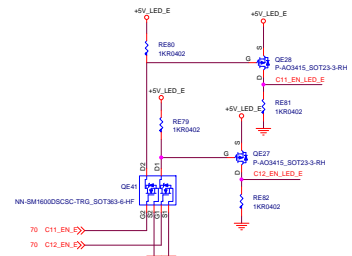
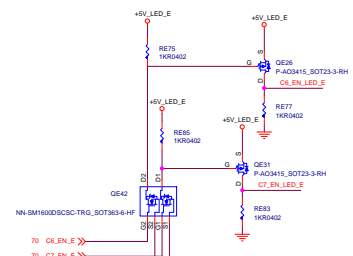
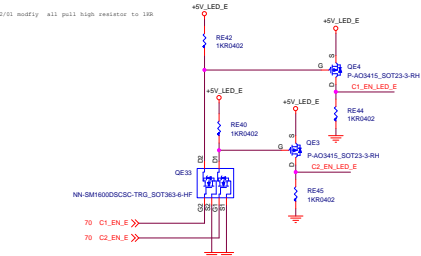
1. The external capacitor protects the device against parasitic resets.
2. The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in Table 56: NRST pin characteristics. Otherwise the reset will not be taken into account by the device.



Confirm Pin 1 position



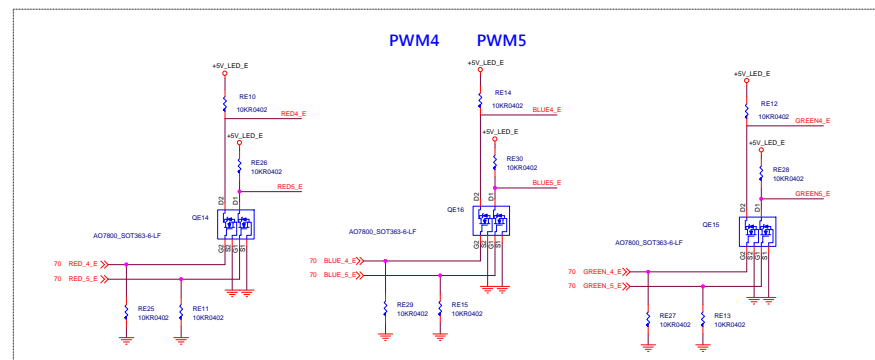
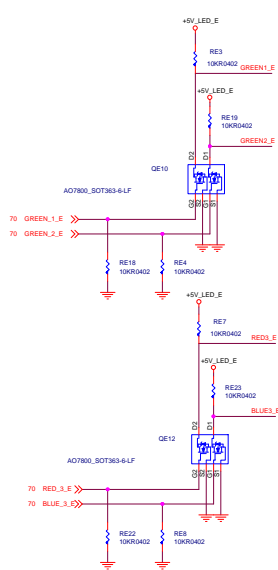
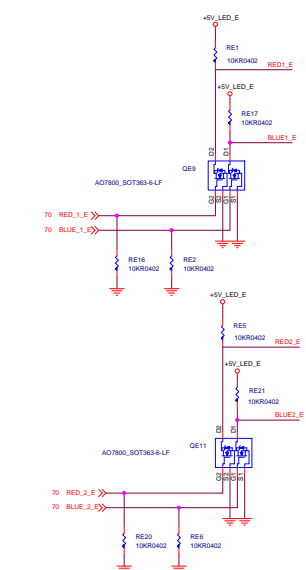
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Size Document Number			
MS-17B6E			
Rev			
DB			
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Sheet 70 of 74			



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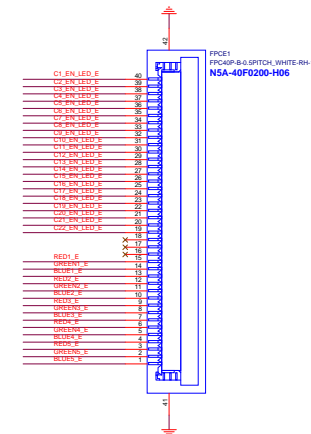
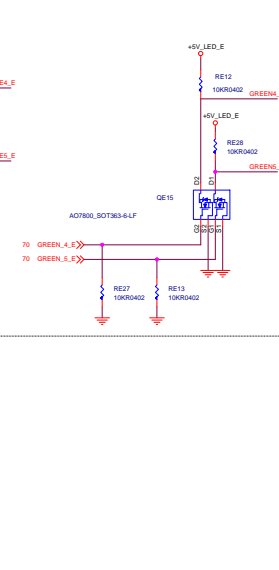
Change C5_EN control, 2017/4/24

PWM1 PWM2 PWM3



PD0-16K6E0B-H73

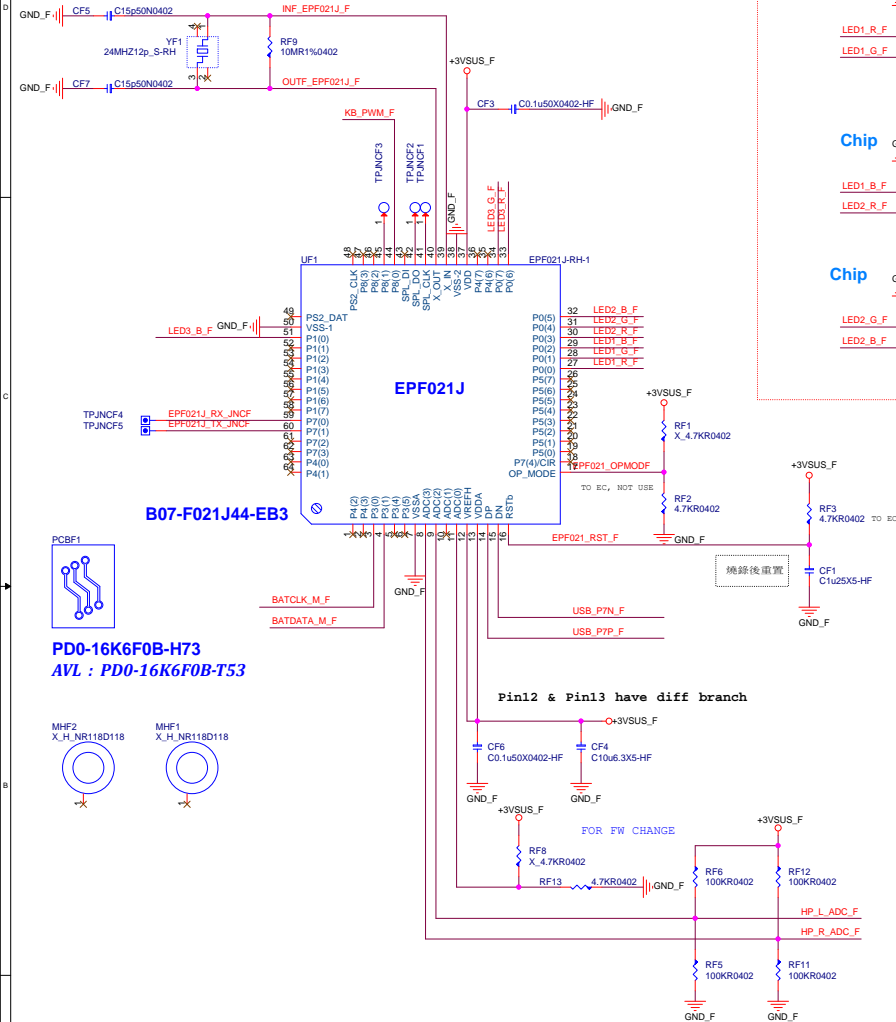
PWM4 PWM5



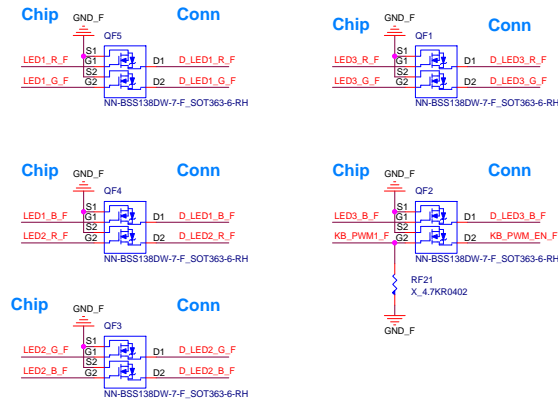
LED 8051 Controller

F PCB 8/21 增加

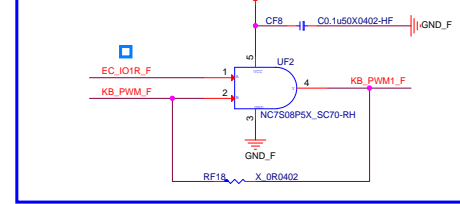
C749 and C750 change to 15pF for 8A



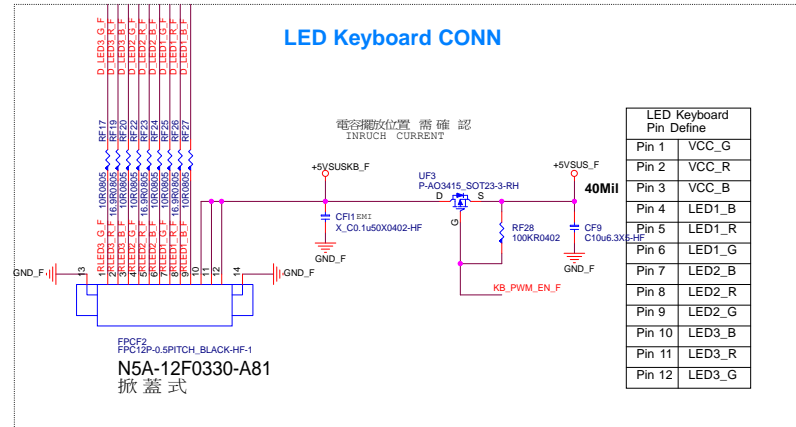
EPF021J Sink current not enough, only using BSS138 (0.22A)



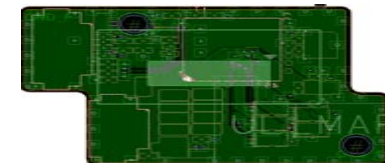
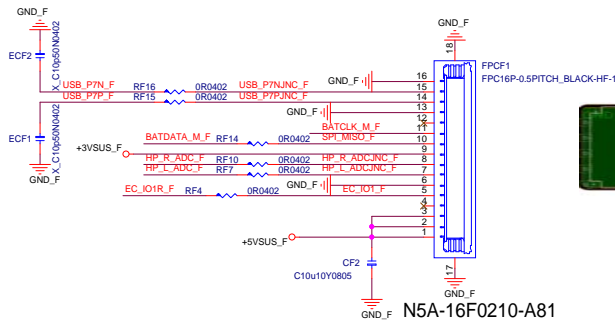
解決 KB開關的問題



LED Keyboard CONN



LED Keyboard Pin Define	
Pin 1	VCC_G
Pin 2	VCC_R
Pin 3	VCC_B
Pin 4	LED1_B
Pin 5	LED1_R
Pin 6	LED1_G
Pin 7	LED2_B
Pin 8	LED2_R
Pin 9	LED2_G
Pin 10	LED3_B
Pin 11	LED3_R
Pin 12	LED3_G



Ref #543611 Chapter40
Figure 40-4. SKL-S Timing Diagram for G3 to S0/M0 (Non-Deep Sx Platform)
Table 40-5. Platform Sequencing Timing Parameters



Ref #543611 Chapter40
Figure 40-6. SKL-S Timing Diagram for S0 to G3 [Non-Deep Sx Platform]
Table 40-5. Platform Sequencing Timing Parameters



History 0A-->0B

16K61 0A BOM CFG: CFG_16K61_G0_S2
17B61 0A BOM CFG: CFG_17B61_G1_S4

P36. R488 Coding 10 ,Change PN

Power Team 9/15 16K6 Change
PC189--> 390pF C11-3911812-W08
PC174--> 1500pF C11-1522812-W08
PC39--> 0.033uF C11-3332512-Y01
PC202--> Stuf f 330uF
PR33-->2.21K R11-2211T22-W08
PR180-->63.4K R11-6342T12-W08
PR178-->41.2KR11-4122T12-W08
PR207-->53.6K R11-5362T12-W08
PR182-->115K R11-1153T12-W08
PR203-->511R R11-5110T12-W08
PR42-->64.9K R11-6492T12-W08
C360.C370.C381.C383--> N.C

Power Team 9/19 PC61 Stuf f
9/20 Q24 D&S Reverse

9/21 P59 PC31 Pull Wrong

9/21 ME SW1 Remove

9/25 P34 R139,R140 Stuf f --> DP Do Not Show

9/27 P21 Purchase 31-25Q8043-W03
Change to M31-25U8002-M24

9/27 P41 R160,R161
Change 75 Ohm-->1K

9/27 P 32 AL37 To GND

9/27 P26 Add Test Pin TP1 & TP2

9/28 P31 For 16K6F 3 colorK/B
R548 No stuff, R549 stuff

9/28 EMI Chage Choke PN.
-> L12-9008150-T19
EL1,EL2,EL3,EL4,EL5,EL6
ELA7,ELA8,ELA9
L6,L7
LI1,LI2,LI3,LI4,LI5,LI6

9/29 P42 PM Jerry Required U40
Change PN: I9C-5302S0C-CL9

10/3 P7 PM_SLP_S3#-->RUN_ON

2017/10/3 :Power Change PN.
1.PL14-->L04-15A7700-M26
2.PEC5 No stuff
3.PR110-->37.4K (R11-3742T12-R01)
4.PR103-->34.8K (R11-3482T12-R01)
5.PL10-->L04-01073F0-M26
6.PR244-->20K (R11-0203T12-R01)
8.PC61 Stuf f
9.1_8V Power soluti on change
(EMI Sever) 16K6_1.0_1002_1V8 Power
P52 PU7-->I9C-P21470C-M03
Add PC242 & PC243
PL8 PN-->L04-47B70G0-M26
ADD PC244-->C11-1042042-W08
PC244 No Stuf f
Add PC245-->C11-1057322-W08
ADD PR295 & CR294,
PN-->R11-0000012-W08 No Stuf f
Add PR292
PN-->R11-0000012-W08


10/11 P46 PM UNSTUFF FPC6 White
Color Keyboard

10/11 P47 PM UNSTUFF FPC7 Finger Print

10/13 P34 DP R186 STUFF, R185UNSTUFF
R143 STUFF

10/13 P59 PC26 STUFF,PR79 STUFF,
PR81 UNSTUFF

9/22 P26 CPU PWROK & PCH_PWROK RedRAW
P53 Change PR183 ==>120K

 MICRO-STAR INT'L CO.,LTD.			
File History			
Size	Document Number		Rev
	MS-16K61/17B61		0B
Date:	Wednesday, October 18, 2017	Sheet	74 of 74